

Simulation-Based Evolutionary Heuristic to Sizing Analog Integrated Circuits

Lucas Compassi Severo, Alessandro Girardi
{lucassevero, alessandro.girardi}@unipampa.edu.br

Federal University of Pampa – UNIPAMPA
Graduate Program on Electrical Engineering
Alegrete – RS – Brazil

Abstract

The goal of this paper is to present a tool for automatic synthesis of analog basic integrated blocks using the genetic algorithm heuristic and external electrical simulator. The methodology is based on the minimization of a multi-objective cost function and a set of constraints in order to size circuit individual transistors. The synthesis methodology is implemented in Matlab and use GAOT (Genetic Algorithm Optimization Toolbox) as heuristic. For circuit simulation we used the Synopsys HSPICE® simulator. As circuit design example, this paper shows the application of this methodology for the design of an OTA Miller for two different fabrication technologies.

1. Introduction

The design automation of analog integrated circuits can be very useful in microelectronics, because it provides an efficient search in the design space, among a set of design constraints, to make it more efficient as possible. Several works have been done in this theme, aiming the development of tools for the automation of time-consuming tasks and complex searches in highly non-linear design spaces [1] [2]. However, as far as we know, there is not a commercial tool capable to perform the synthesis of analog circuits with optimum results in a feasible time. An important improvement in the analog design could be the automation of some design stages, such as transistor sizing and layout generation [5], maintaining the interaction with the human designer. The large number of design variables and the consequent large design space turn this task extremely difficult to perform even for most advanced computational systems. Therefore, it is mandatory the use of artificial intelligence with great computational power to solve these problems.

In this context, we propose an automatic synthesis procedure for basic analog building blocks which can size transistors width (W) and length (L) with efficient time and ordinary computational resources. The synthesis procedure has as main strategy the global search using genetic algorithm and the evaluation of circuit characteristics through the interaction with an electric simulator. The Genetic Algorithm (GA) is an heuristic idealized in 1975 by scientist John Holland inspired by principles of natural evolution proposed by Charles Darwin. This evolutionary heuristic is very used for automatic design of integrated circuits [3].

This work is organized as follows: section 2 shows the description of the proposed methodology; section 3 presents the application of the methodology in the design of a specific analog block - OTA Miller - with circuit description and final results; finally, section 4 shows the conclusion.

2. Simulated Based Evolutionary Heuristic Methodology

The proposed methodology is based on the reduction of a multi-objective cost function for a specific analog block. This cost function is dependent on the circuit electrical characteristic and is implemented as an equation in terms of circuit variables. The electrical characteristics can be power consumption, silicon area, voltage gain, etc, or a combination of these. The optimization is based on the minimization of a cost function and a set of constraints. This minimization is performed by genetic algorithm with values provided by electrical simulations through an external electrical simulator.

The genetic algorithm is an heuristic for non-linear optimization based on the analogy with biologic evolution theories [3]. It is a non-deterministic algorithm and it works with a variety of solutions (population), simultaneously. The population is a set of possible solutions for the problem. The size of the population is defined in order to maintain an acceptable diversity considering an efficient optimization time. Each possible solution of population is denominate chromosome, which is a chain of characters (gens) that represent the circuit variables. This representation can be in binary or float numbers. The quality of the solution (fitness) is defined by an evaluation function (cost function).

In analog integrated circuits design an important stage is the circuit sizing, where the transistor dimensions (channel width and length) are obtained. This task can be done manually using simplified equations that describe the transistors size in terms of the circuit specifications. Due to equations simplicity, results may not describe the real circuit behavior. Another characteristic is that in these equations, in general, the transistors are operating in strong inversion region, limiting the optimization for low power circuits.

In order to solve this task and explore the circuit design space in order to find optimized feasible solutions (solutions that reach design constrains), evolutionary heuristics, such as genetic algorithms, with an electrical simulator, can be a good alternative.

In Fig. 1 is shown the automated design flow using genetic algorithm. The methodology has the tool settings, design objectives and technology parameters as inputs. In tool settings the genetic algorithms, circuit netlist, simulation options and variables bounds are configured. In the design objectives the set of values required to the circuit specifications and the specifications that will be optimized are configured.

The first genetic algorithm step is the population generation, created randomly. To get the population fitness all generated solutions are evaluated using a commercial electrical simulator and a multi-objective cost function. Based on evaluation and selection method the parent chromosomes are selected for generating new chromosomes (solutions). The new chromosomes are created through crossover and mutation - analogy with biology. The crossover (recombination) is responsible for generating one or two solution through two chromosomes of populations. The mutation is a random change in some gen (variable) of a chromosome. A lot of alternative are possible for crossover and mutation functions [4].

The next step is to evaluate new solutions (chromosomes), using again the electrical simulator and a multi-objective cost function. Based on these values, new chromosomes are introduced in the population. At the end of the iteration, the stopping condition is tested and, if true, the optimization is finished. Otherwise, new parents are selected and the process is repeated. The stopping condition can be the number of generations (iterations), minimal variation between variables or cost function, or others.

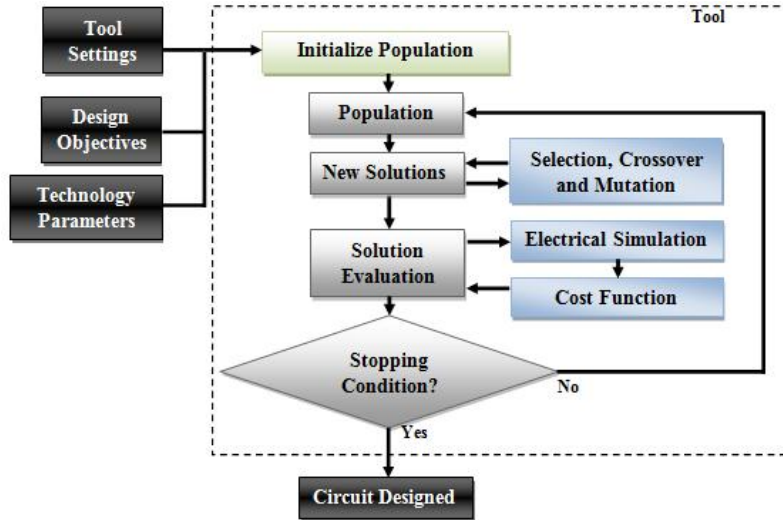


Fig. 1 – Design flow for the analog synthesis using genetic algorithms.

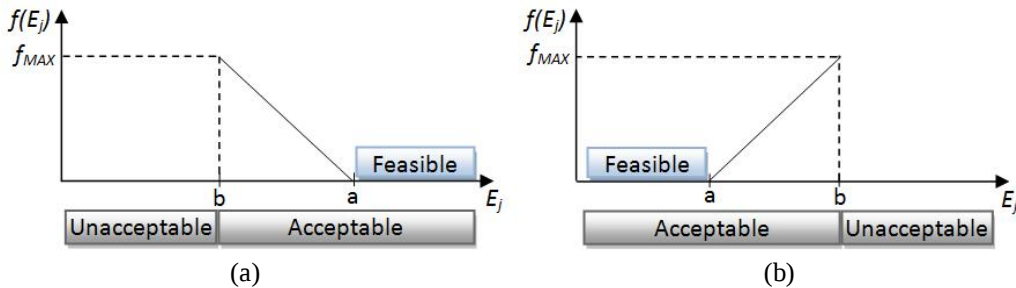


Fig. 2 – Cost function performance metric, (a) minimum required value specifications and (b) maximum required value specifications.

In this methodology the optimization procedure has a multi-objective cost function according to Eq. 1. In this equation E_i , is the specification that must be optimized. There can be n specifications according to designer needs. In this paper we used power dissipation and gate area of circuit. $f(E_j)$ is the performance metric dependent on the specifications that are constrained in minimum or maximum values. This function is shown in Fig. 2 and is dependent on the type of specification (minimum – Fig. 2 - a - or maximum – Fig 2. b -

required value) and the bounds of feasible and acceptable solutions a and b , respectively [7]. P_{O_i} and P_{R_i} are the weights parameters for each specification.

$$f_c = \sum_{i=1}^n P_{O_i} \cdot E_i + \sum_{j=1}^m P_{R_j} \cdot f(E_j) \quad (\text{Eq. 1})$$

An important characteristic of these cost functions is that non-feasible solutions are admitted as a possible circuit solution. As shown in Fig. 2 the unfeasible solutions has a $f(E_j)$ value that depend on the distance between an “a” required value and the measured specification value (E_j). It is done because a bad solution can be a path to a good solution and if these solutions are ignored the algorithm cannot explore this region effectively [5].

The synthesis tool developed in this work is implemented in Matlab® and use the Synopsys Hspice® simulator to perform the circuit electrical simulation. For the execution of genetic algorithm, we adopted GAOT (Genetic Algorithm Optimization Toolbox), an implementation of GA for Matlab developed by [4].

3. OTA Miller Automatic Sizing

As a design example using the proposed methodology, described in this paper, we used a two-stage CMOS Miller operational transconductance amplifier (OTA). The schematic of this amplifier is shown in Fig. 3. The Miller OTA is composed by an input differential pair and a current mirror with active load in the first stage. The second stage is composed by an inverter amplifier. Between the first and second stages is connected a compensation capacitor for stability purposes [6].

The main specifications of this circuit are low frequency gain (A_{v0}), slew rate (SR), phase margin (PM), input common-mode range (ICMR), output swing (OS), power consumption and gate area.

In the automatic synthesis are defined as free optimization variables the transistor widths (W) and lengths (L) and the bias current source (IBIAS). In the circuit of Fig. 3 there are the following equalities: $M1=M2$, $M3=M4$, $M7=M8$. So, there are eleven design free variables to solve in the circuit. Fig. 4 shows the genetic algorithm float chromosome for this problem.

For this design the population is set to 100 individuals. As crossover type we used arithmetic and heuristic crossover simultaneously and as mutation function we used non-uniform and uniform mutation simultaneously [4]. As selection function we chosen normalized geometric selection. As stopping condition is it considered a number of 100 generations. The bounds for variables selected as follows: for W a range of W_{min} (that depends on technology) to $1000 \mu m$, and for L a range between L_{min} (also dependent on the technology) to $100 \mu m$ and for IBIAS the range between $1 \mu A$ and $300 \mu A$.

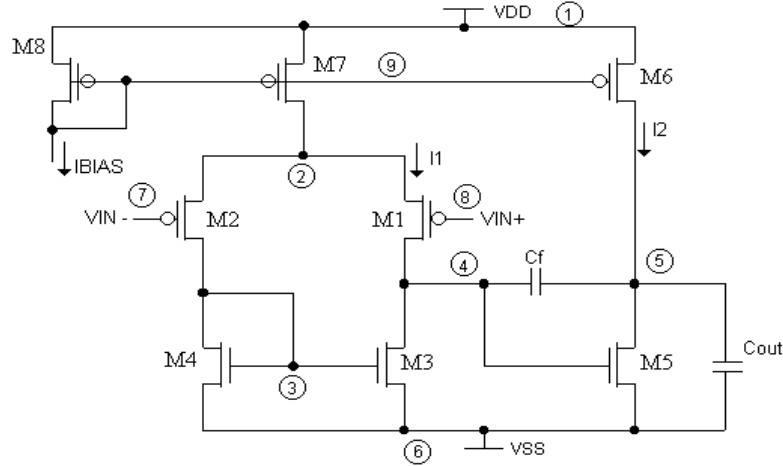


Fig. 3 - Schematics of a two-stage Miller operational transconductance amplifier (OTA)

W_{M1}	L_{M1}	W_{M3}	L_{M3}	W_{M5}	L_{M5}	W_{M6}	L_{M6}	W_{M7}	L_{M7}	I_{BIAS}
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Fig. 4 - Genetic algorithm chromosome representation for this problem.

To design the circuit we used two different technologies: AMS $0.35 \mu m$ and XFAB $0.18 \mu m$. The goal of this choice is to verify if the technology that the circuit will be implemented has influence in the design procedure.

The required specifications values are shown in the second column of Tab. 1.

The tool was executed and the reached values are shown in the third and fourth columns of Tab. 1 for the XFAB $0.18 \mu m$ and AMS $0.35 \mu m$ technologies, respectively. In these results it is possible to see that all

specifications required were met. Analyzing the best result, minimum power dissipation and gate area, it is possible to see that the best result is obtained with the XFAB 0.18 μm technology, with the power dissipation about 45% less than AMS 0.35 μm technology and the gate area of the circuit about 80% less than 0.35 μm technology. The execution time was 7 minutes faster than the execution with AMS 0.35 μm . This result is justified because the XFAB 0.18 μm has smaller transistor sizes and voltage supply. These specifications are important to find a circuit with reduced size and low power dissipation. In the Tab. 2 are shown the design parameters for these executions.

Tab. 1 – Design results of the technology Comparison

Specifications	Required	XFAB 0.18 μm	AMS 0.35 μm
A_{v_0} (dB)	≥ 70	85.71	73.88
GBW (MHz)	≥ 1	1.80	1.14
PM ($^\circ$)	$\geq 60^\circ$	72.35	85.87
SR (V/ μs)	≥ 1.00	1.00	1.02
ICMR+ (V)	≥ 0.4	0.62	1.30
ICMR- (V)	≤ -0.4	-0.87	-1.62
OS+ (V)	≥ 0.8	0.82	1.50
OS- (V)	≤ -0.8	-0.89	-1.64
Pdiss (μW)	$\downarrow$	18.05	33.00
Gate Area (μm^2)	$\downarrow$	108.39	546.21
Exec. time (min)	-	52.0	45.0

Tab. 2 – Design parameters obtained with proposal methodology.

Parameters	XFAB 0.18 μm	AMS 0.35 μm
W1/L1 ($\mu\text{m}/\mu\text{m}$)	6.73/0.64	3.63/2.45
W3/L3 ($\mu\text{m}/\mu\text{m}$)	13.59/0.80	34.97/3.07
W5/L5 ($\mu\text{m}/\mu\text{m}$)	51.15/0.24	215.13/0.64
W6/L6 ($\mu\text{m}/\mu\text{m}$)	97.81/0.39	83.28/0.81
W7/L7 ($\mu\text{m}/\mu\text{m}$)	34.78/0.38	20.11/2.72
IBIAS (μA)	10.02	10.00
Circuit Constants		
VDD (V)	1.8	3.3
Cout (pF)	10	10
Cf (pF)	0.3	0.3

4. Conclusion

The proposed methodology using simulation-based evolutionary heuristics for sizing analog integrated circuits presented good results in a reasonable computing time. Genetic algorithms are very suitable for analog design automation because the convergence of the final solution is not directly dependent on initial solution, and it is not necessary a great experience by the human designer about the circuit characteristics.

The methodology was demonstrated in two technologies, where it is possible to see that it can explore different design spaces and can be used to make comparisons of different fabrication technologies.

As future work, we intend to compare the solution obtained by GAs with other optimization heuristics, in order to analyze the algorithm parameters that contribute to best solutions. Also, we can explore the use of electrical simulators from different vendors, expand the methodology for other analog basics blocks and insert an analysis of parameters variability in fabrication process.

5. Acknowledgments

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6. References

- [1] Martens, E., Gielen, G. G., Classification of analog synthesis tools based on their architecture selection mechanisms, VLSI Journal Integration, vol. 41 Issue 2, February, 2008.
- [2] Phelps, R., Krasnicki, M., Rutenbar, R.A.; Carley, L.R.; Hellums, J.R., Anaconda: simulation-based synthesis of analog circuits via stochastic pattern search, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 19, Is. 6, p.703-717, 2000.
- [3] R. S. Zebulum, M.A.C. Pacheco, M.M.B.R., Vellasco, "Evolutionary Electronics: Automatic Design of Electronic Circuits and Systems by Genetic Algorithms", USA: CRC, 2002.
- [4] Houck, C., Joines, J., and Kay, M., "A Genetic Algorithm for Function Optimization: A Matlab Implementation", NCSU-IE TR 95-09, 1995.
- [5] Bo Liu, Francisco V. Fernández, and Georges G. E. Gielen, Efficient and Accurate Statistical Analog Yield Optimization and Variation-Aware Circuit Sizing Based on Computational Intelligence Techniques, IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, vol. 30, no. 6, June 2011, pp.793-805.
- [6] P. E. Allen and D. R. Holberg, "CMOS Analog Circuit Design", Oxford University Press, Oxford, second Edition, 2002.

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- [7] Barros, M. F.M., Guilherme, J. M. C. and Horta, N. C. G., “Analog Circuits and Systems Optimization Based on Evolutionary Computation Techniques”, Studies in Computational Intelligence, Volume 294, Springer, 2010.