

Simulation of SET Faults in a Voltage Controlled Oscillator

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Abstract

In Integrated Circuits (ICs), the faults can lead to permanent, transient or intermittent errors. In the case of transient faults, they take place for a very short time. These faults can lead from small unexpected changes in the results or even in the circuit complete and permanent failure. One of transient fault is known as Single-Event Transient (SET), which occur in combinational logic and analog circuits typically. The study of the behavior of a circuit under fault is important to choose the protection techniques and measurement of susceptibility to the type of fault inserted. Nowadays, the fault simulation is an important step in any IC design. Predicting the behavioral faults is essential to ensure that the design is well implemented. During simulation various problems can be detected and corrected. We present a toolkit to simulate the effect that occurs when a SET failure source is inserted in a 250nm CMOS Voltage Controlled Oscillator (VCO) using National Instruments LabVIEW. The results of these simulations were compared with results obtained in the laboratory by W. Chen et al. in 2003.

1. Introduction

With the advancement of technology and the shrinking of the device sizes, the integrated circuits become more susceptible to errors due to radiation effects. The radiation sources may come from space (solar flares, Van Allen belts, solar wind or cosmic rays) [1], or from radioactivity or electromagnetic sources generated on Earth. Once the circuit is exposed to a radiation source, it can have a logical value changed, altering the characteristics of the circuit or even permanently damaging the device, depending on the amount of radiation to which the circuit is exposed. These are the main reasons why it is important and necessary to predict the Faulty ICs behavior due to these phenomena. Transient faults, which are one of the many types of failures due to radiation, are failures that last for a short period of time. These failures can go from low magnitude noise to pulses big enough to produce permanent damage in electronic devices. There are also cumulative effects that make the equipment fail gradually until complete loss. Among these faults are SETs, which are produced by particles that hit the reverse-biased PN junctions, causing an abnormal current flow.

Analog circuits are also affected by the SET, you need only to insert a pulse of longer duration and high charge. A Voltage Controlled Oscillator (VCO) is a very important analog circuit for radio frequency and communications, which produces an oscillating signal and a variable voltage controls its frequency. The principle of operation of this circuit is the Barkhausen Criterion, and the use of a pair of transistors in Crossed Pair configuration to produce a negative resistance that keeps the Tank circuits oscillating [2]. One of the most sensitive parts of this circuit is the twisted pair transistors, which are equal with transconductance g_m . If occurs a transient pulse current due to a particle, this will vary the value of g_m making that the Barkhausen Criterion is not satisfied. Then the VCO will not oscillate correctly, i.e. no constant amplitude. To simulate this phenomenon it is used a pulsed laser to simulate the impact that a heavy ion that causes a transient over 30pC, which is sufficient to simulate a SET in this circuit [3].

National Instruments LabVIEW is a graphical programming framework used in the industry as an interface between users and tools. It is a graphical and parallel language, easy to learn and to debug, which makes it easy for engineers and scientists, even those with limited programming skills [4], [5]. Programming with LabVIEW remembers the wiring of electrical circuits, making it easier to follow the data flow in the program, rather than with a text circuit description. The program in LabVIEW is called Virtual Instrument (VI). Each VI has an user interface or Front Panel (FP) and a Block Diagram (BD) where programming is done.

The commercial electrical simulators are not really prepared to insert faults in ICs. The aim is to generate a toolkit in LabVIEW 8.20 that can be used to simulate SETs caused by ions or lasers pulsing on a 250nm CMOS VCO circuit and to compare with the experiment reported in [3].

The paper is organized as follows: section 2 describes the developed toolkit. Section 3 shows the result obtained with the experiments, section 4 shows the conclusion and the future works are in section 5.

2. Developed Tools

The developed VIs includes full circuit simulations with transistors, capacitors, varactordiods, and so on. This was done to facilitate programming in LabVIEW (hierarchical) [6]. The simulations made with these tools are at Logic Gate Level [1]. The transistor simulation in this toolkit is based on a MOS Transistor quadratic model. In this model, the drain current I_D have different equations to model the different MOS operation regions [3], [7]: Sub-Threshold, Resistive and Saturation regions.

The tool **NMOS Current Mirror PtByPt.vi** simulates a Current Mirror made with NMOS transistors and PMOS Pull-Up. Its VI and schematic are shown in figure 1. The **Iset** current, **Vout** voltage and adequate transistor sizing is necessary to fix the **Iout** current. The **Vref** output shows the Mirror transistors gate-source voltage. The **Req** output is the drain-source resistance of mirror transistors. To set the technological and geometrical parameters of the NMOS transistors of the mirror and PMOS pull-up it is necessary to define the values of the corresponding clusters.

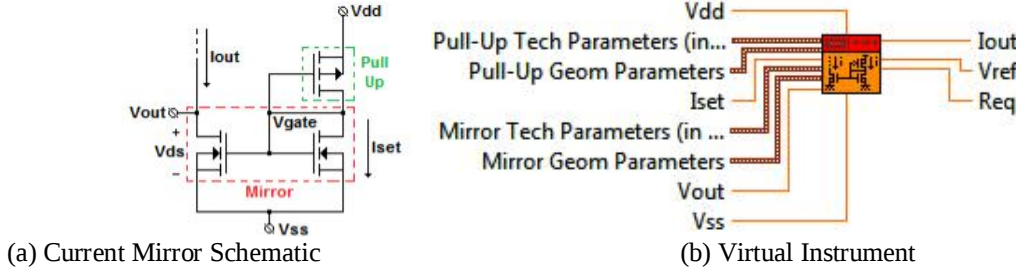


Fig. 1 – NMOS Current Mirror PtByPt.vi

The tool **Tank PtByPt.vi** is a VI that performs a functional simulation of Tank Circuit. It is based on a capacitance and inductance in parallel. Its VI and schematic are shown in figure 2. In order to “tune” the Tank the **Vtune** input must be used with a double precision number between 1 and 1.8V to set the Tank capacitance between 1 and 500 pF.

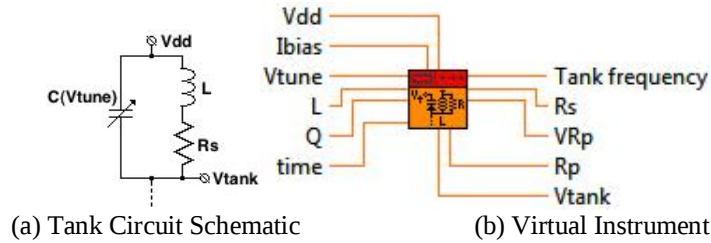


Fig. 2 – Tank PtByPt.vi

The tool **NMOS Cross Pair.vi** simulates the behavior of a crossed transistor pair to generate a negative resistance [2]. This configuration is the base of the oscillators. With this VI is possible to insert a SET fault to observe the behavior of a circuit based on this arrangement (such as VCOs). Figure 3 shows the VI and the schematic of the tool, which is used with two Tank Circuits defined in the VI **Tank PtByPt.vi**.

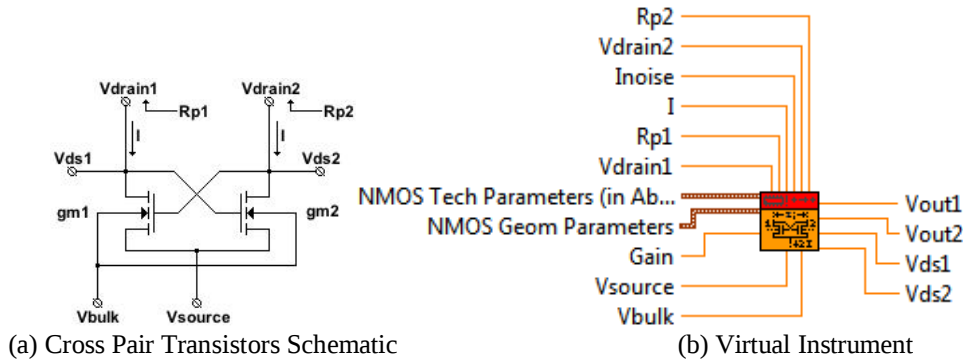


Fig. 3 – NMOS Cross Pair.vi

3. Simulation and Results

In this case, the simulation of a 250nm VCO circuit is affected by a SET pulse with a charge of 37.125pC using the developed tools and others related in [6], e.g. **SET.vi** and **PMOS Active Load.vi**. Alpha particles which impact on analog circuits contributes very little equivalent charge (50fC approximately), which are interpreted as short-term pink noise. To observe the effects of these faults in these circuits it is needed to simulate long pulses and charges greater than 10pC.

A VCO is an analog circuit that generates a sinusoidal signal whose frequency depends on the tuning voltage value (usually this value is smaller than the circuit bias voltage). The VCO circuit is shown in Figure 4. This circuit is based on the use of an arrangement of crossed pair of transistors (formed by transistors M1 and M2) and the Tank Circuits. It also uses a transistor in active resistor configuration (M3) and a current mirror circuit (formed by transistors M4, M5 and M6).

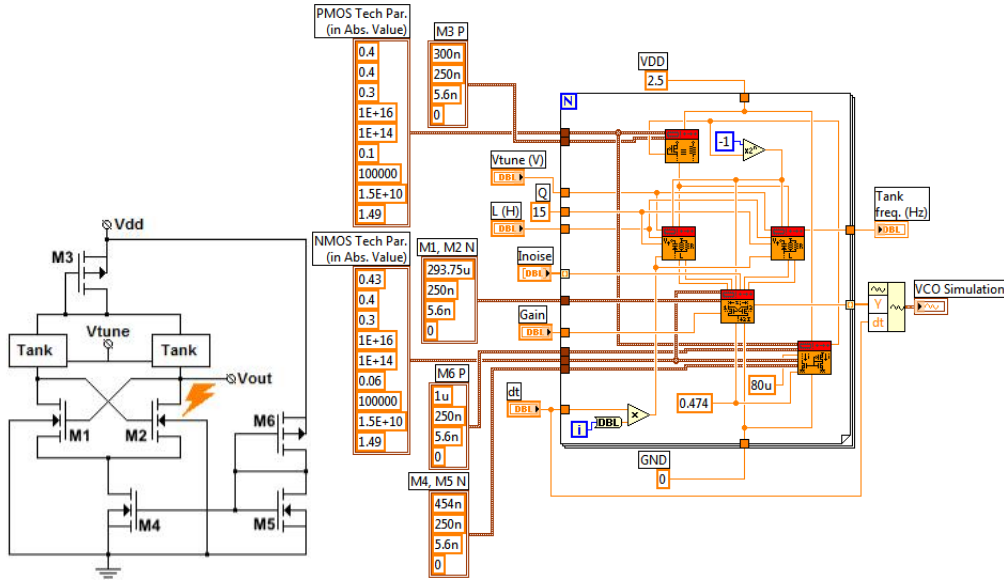


Fig. 4 – VCO Schematic with Fault

Fig. 5 –BD of VCO circuit simulation affected by a Laser pulse

To this simulation an inductance of 10nH is used for each Tank Circuit. The tuning control voltage was set to 1.79V. This generates a sinusoidal signal of 1.15GHz. The asynchronous Laser pulse was simulated using a 37.125pC SET transient pulse. This pulse is applied to the transistor M2 in figure 4[3]. The BD of this simulation is shown in figure 5. The figure 6 shows the results of the simulation, which is compared with results obtained by [3] (shown in figure 7).

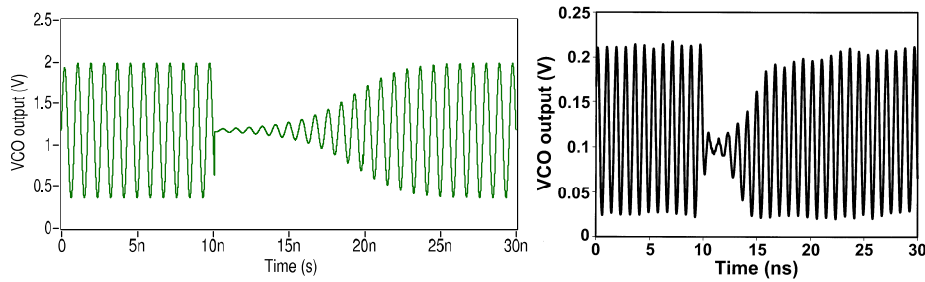


Fig. 6 –VCO circuit simulation affected by a Laser pulse Fig. 7 –Results obtained by Chen et al. (x10) [3]

It is observed in figure 6 that the simulation made using the tools developed in this work is very similar to the experimental results shown in Figure 7. There is also a study about the Fourier spectrum of the signal with and without SET pulse injected to observe the Fading Signature. By the simulation, it has been determined that the broadening of the frequency spectrum corresponds to a temporary disruption in the oscillating VCO output [3]. Moreover, the broadening correlates to a longer amount of time where the signal in time domain is disrupted. The Fading Signature indicates the effect of the total charge deposited on the device and gives an idea of Linear Energy Transfer (LET) magnitude of the incident particle. Figure 8 shows the simulated spectrum of the VCO, showing the influence of the VCO transient pulse, from 0 to 100pC. The increase spreads the spectrum of the signal near to the oscillation frequency. This phenomenon depends on the charge injected into the VCO. One can see that the failure becomes significant from a charge of 90fC (Critical Charge) injected by a SET with ps and ns [1]. Figure 9 shows the same analysis performed with SINAD Analyzer VI [8]. This LabVIEW tool contains a THD Plus Noise analysis, which contains the measured total harmonic distortion plus noise. THD Plus Noise is defined as the ratio of the RMS energy of signal less the energy in the fundamental to the RMS energy of signal. For this case, for THD Plus Noise 10%, occurs the VCO critical charge.

4. Conclusions

A simulation of a 250nm CMOS VCO was done to observe the effects of a SET on this type of circuit.

The Fading Signature and THD Plus Noise are useful tools to predict what will happen in an oscillator circuit when it is affected by a transient pulse. The analysis of these features can also predicts the level of harmonics that will occur in the circuit and the critical charge necessary to generate faults in these circuits.

It was found that LabVIEW is an excellent tool for simulation and analysis of physical and electrical phenomena. The tools provided by this programming environment are very helpful in data analysis, 3D graphics and Fourier spectrum. It should be observed the accuracy of the data and equations used in simulations.

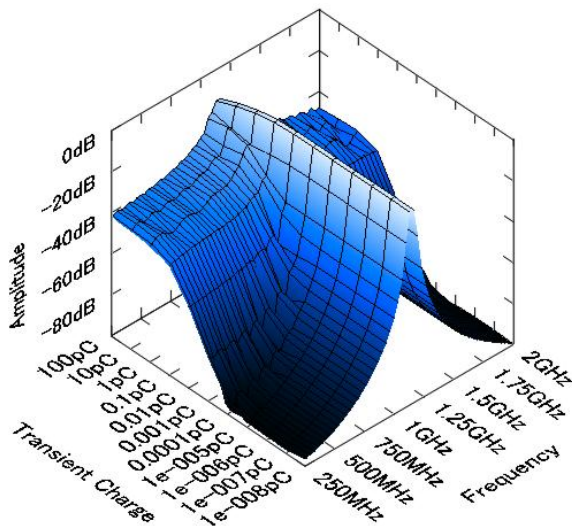


Fig. 8 – VCO Fading Signature

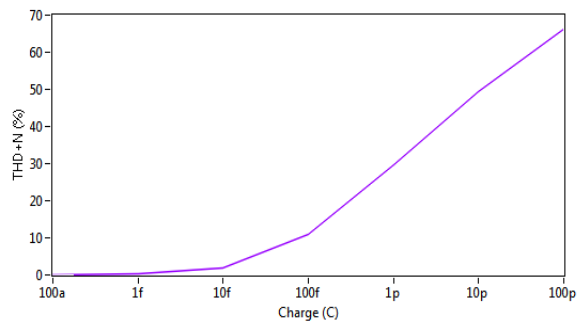


Fig. 9 –VCO THD Plus Noise Analysis

5. Future Work

Further studies should be made concerning capacitors, inductors, active resistors, and current mirrors with transitory faults to add these features to the corresponding VIs. It is necessary to analyze some cases where these devices are affected in the VCO.

VIs for the simulation of failures in other CMOS analog circuits such as differential pairs, cascode amplifiers and Miller, etc. will be further developed, in order to provide coverage to as many potential cases of transient faults as possible.

VIs that can also simulate the effects of total ionization dose will be developed to generate a unified model with the obtained for transient fault simulation.

Will be create VIs that perform their own analysis functions for these tools can be run on any version of LabVIEW, from the 8.20 student version onwards.

6. Referências

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