# Full Adders Architectures Evaluation for 32nm Technology

**[2]Augusto Silva, [2]Ingrid Machado [1,2]Cristina Meinhardt [2,3]Paulo F. Butzen**
augustoneutzling@inf.ufrgs.br, ingridecomp@gmail.com, {cristinameinhardt, paulobutzen}@furg.br

**[1]PPGC – Universidade Federal do Rio Grande do Sul – UFRGS**
**[2]Centro de Ciências Computacionais – Universidade Federal do Rio Grande – FURG**
**[3]PGMICRO – Universidade Federal do Rio Grande do Sul – UFRGS**

## Abstract

*This paper presents an evaluation of several full adder architectures in order to verify which one is the most appropriate for a particular use. The selected architectures were the most widespread according to literature, which are: CMOS, CPL, Hybrid, TFA, TGA and 14T. A 32nm predictive technology was used to describe the architectures. Electrical simulations were performed and the delay, dynamic and static power were measured. Results show that the CPL is a good option for a delay constraint, when the circuit stays a long time on standby, because has the lowest static power consumption, and the CMOS, TFA and TGA consume less dynamic power.*

## 1. Introduction

The complexity of the portable devices is growing in an exponential way. However, the batteries capacity has not evolved in the same velocity, compromising the autonomy of products that make use of them. The devices scaling allowed the greater integration mentioned before, and with several architectural techniques, the performance has become so high that it is enough for most users. However, the decrease of the power consumption has not evolved in the same way, making this restriction the greater challenge of the new technologies. By the growing number of portable devices, this challenge becomes even more important [1][2][3].

One of the most important parts of any electronic system is the adder circuit, a digital circuit which sum bits. The adder cell function itself does not sound complex. But, when analyzed how many times a processor executes the sum operation, the importance of this circuit in system is verified. Adders are the base of many others operations like as subtraction, multiplication and division. It is the main cell of the arithmetic logic units (ALUs). The ALUs are responsible for performing arithmetic operations on data and addresses, making logical decisions, such as deflects and procedures calls [4].

Due to the value of the adders circuits, several transistors architectures were proposed as well as numerous works evaluate these adders [5-10]. The main architectures studied are the CMOS, CPL, Hybrid, TFA, TGA and 14T. They appear in the majority of such articles and the circuits of each one are presented in fig. 1.

The main objective of this work is to establish a comparison between those six adders architectures in a nanometer technology. Almost all the previous works brings only an evaluation of dynamic power and delay. However, in nanometer technologies, the leakage currents turn the static power an important part in the total power consumption. In this sense, this work evaluates delay information and both dynamic and static power data. Besides, it is important to verify if the results found for older technologies, as in [7] [8] [11] [12], are maintained or changed when compared to nanometer designs.

## 2. Adders Architectures

There are many ways to implement the sum function. It can be generated by the simplification of the function itself and by different ways to implement each logic gate. After a review of several articles that evaluate adders circuits [2-13], six adders circuits were chosen to be explored in this work. The circuits are the CMOS, the CPL, the hybrid, the TFA, the TGA and the 14T, which are shown in fig. 1. This chapter presents a brief description of these adders.

CMOS is the standard adder architecture. It is based in the CMOS logic family which has complementary pull-up and pull-down transistor networks. It has a high driven capacity [6][11][13]. The “Complementary Pass-transistor Logic”, CPL, is another well known adder. It uses the concept of pass transistors. It provides the output and its complement, high performance, strong output signals and a good driven capacity [4][5] .The Hybrid is known as a mix of the two logic families in order to optimize its performance and power consumption. The circuit works well in low voltages, because it has a strong output signal [7][9].

The TGA (Transmission Gate Full Adder) is based on the transmission gates theory, which consists of a PMOS and a NMOS transistors connected in parallel, being a special type of pass transistor. TGA has the advantage of not showing many problems with low voltage [7, 10]. The TFA (Transistor Function Full Adder) is also based in the transmission function theory. It uses pull-up and pull-down paths to make the inverters, and utilizes some transmission gates for the rest of the logic obtaining efficient implementations for the XORs and NORs [6][7][12]. The main disadvantage of the TFA and the TGA is the lack of the driven capacity, suffering much signal degradation when cascaded [7 ,10]. The 14T adder has the advantage of consuming only a little area. 14T uses the function XOR combined with the transmission gate function and, as the TFA, implements a complementary pass transistor logic to load the output[7][13].

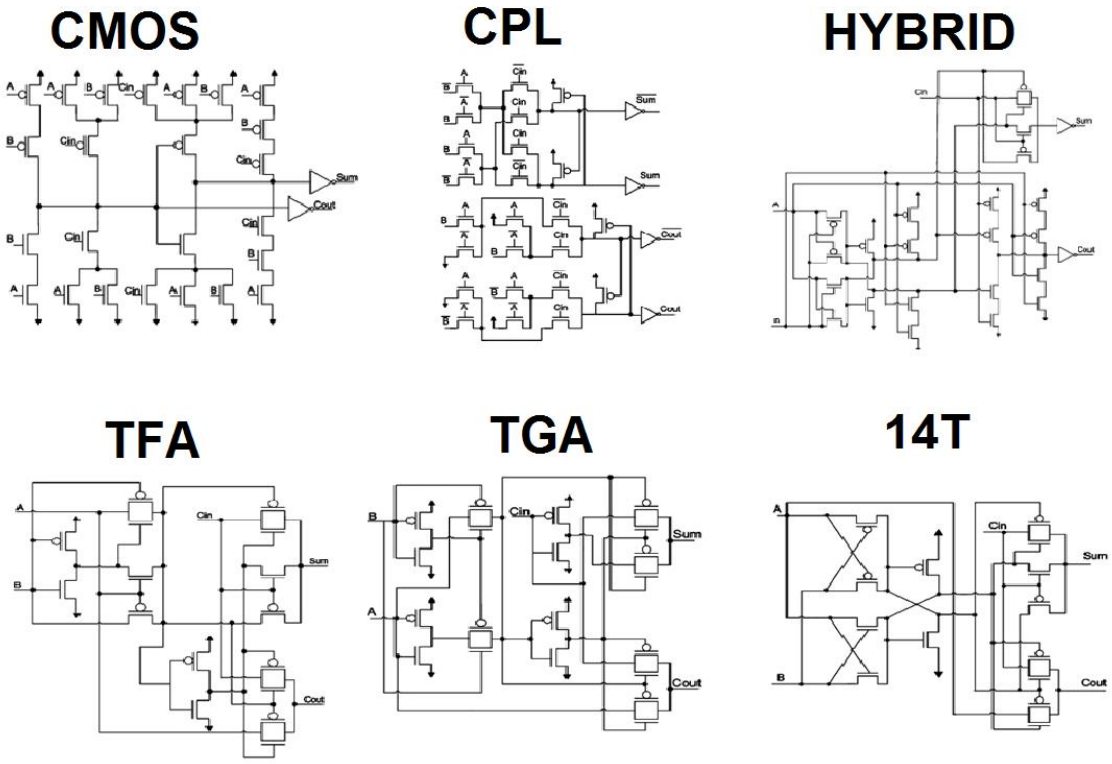


Fig. 1 – Evaluated Full Adders Architectures

## 3. Methodology

To allow a complete comparison between the different adder circuits, the delay, dynamic and static power of all six architectures were measured. A 32nm predictive technology was used to describe the circuits and the electrical simulations were performed in NGSPICE simulator. The sizing used was the same suggested in [9] which is also utilized in [6], [7-9]. The supply voltage was 0.9V, the nominal voltage for the 32nm technology [14].

The power of each transition was obtained by the equation (1), and the dynamic power was calculated from the average between the values of the powers from 24 possible transitions of 1 bit. The delay was also an average between the 24 propagation delays. Between the sum bit delay and the carry bit delay, prevailed always the biggest. Buffers were used in the input and the output, to simulate a real circuit, as if each block was in a chain of full adders, and outputs connected to flip-flops.

$$P_{avg} = \frac{1}{T} * \int_0^T I(t) * U(t) * dt \quad (1)$$

To calculate the static power, the 8 logical combinations of possible entries were simulated and the average is presented. The PDP is the product of the dynamic power by the delay, and was calculated from the results of these two parameters. Area was analyzed considering only the number of transistors.

# 4. Results

Tab. 1 presents the values obtained through simulations. The area was analyzed only in the number of transistor, and a more accurate analyze will be performed at future works. The graphs of the fig. 2 show the normalized results of the dynamic power, delay, PDP and static power, respectively. By the simulations results was observed that the CPL architecture has the higher dynamic power consumption. One reason for this is the fact that CPL switching has to generate transitions for the outputs and for the complementary outputs. Following, the 14T and the Hybrid consume more than the CMOS. TFA and TGA adders present a low consumption, but they present much signal degradation when cascaded,.

In relation to the delay, the hybrid presented the worst values, followed by the 14T. The TFA has largest delay than the CMOS and the CPL and the TGA have the lowest delay. It was observed that the Hybrid presents the worst PDP value, followed by the 14T and the CPL. CMOS presented a better result. The TFA and the TGA presented the best PDP values.

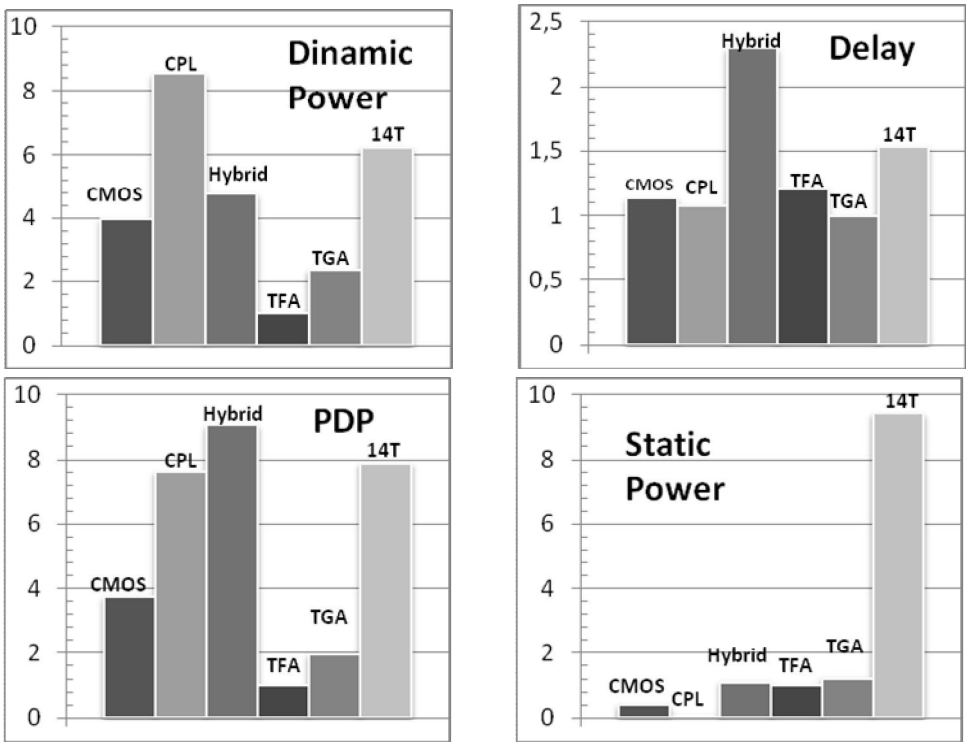


Fig. 2 - Standardized Results

Tab 1 - Simulation Results

| Adder | Dynamic Power (fW) | Delay (pS) | PDP (yJ) | Static Power (nW) | Area (# of transistors) |
|---|---|---|---|---|---|
| CMOS | 1,37 | 33,88 | 0,05 | 10,74 | 28 |
| CPL | 2,94 | 32,08 | 0,09 | 1,83 | 32 |
| Hybrid | 1,64 | 68,50 | 0,11 | 29,16 | 26 |
| TFA | 0,34 | 35,97 | 0,01 | 26,30 | 16 |
| TGA | 0,82 | 29,83 | 0,02 | 32,06 | 20 |
| 14T | 2,14 | 45,78 | 0,10 | 248,33 | 14 |

The analysis of the static power consumption shows that the CPL presents the lowest consumption, followed by the CMOS. The hybrid consumes more than the TFA and less than the TGA. The 14T presents a high static power consumption. The main reason is that for the combination of the sum Cin=1, A=0 and B=0, the consumption is a hundred times greater than in the other cases, which leads the average up.

# 5. Conclusion

The data analyses allow identifying which adders are more suitable for a particular purpose, when designing an integrated circuit in 32nm technology. If the main design objective is to reduce power consumption in a circuit that uses adders several times, the TFA, TGA and CMOS are the most suitable. However, if delay is a critical design constrain, CPL is a good option, together with the TFA. And if the adder circuit will be a long time on standby, the CPL and the CMOS are the most suitable. The 14T and the hybrid are not good choices for this technology, for any objective.

# 6. References

[1] WESTE, N. H., & HARRIS, D. (1993). CMOS VLSI Design – A Circuits and Systems Perspective.

[2] L. Sun, J. Mathew, D. K. Pradhan, and S. P. Mohanty “Statistical Blockade Method for Fast Robustness Estimation and Compensation of Nano-CMOS Arithmetic Circuits” nternational Symposium on Electronic System Design, 2011

[3] T.Kowsalya “Tree Structured Arithmetic Circuit by using different CMOS Logic Styles” ICGST-PDCS, Volume 8, Issue 1, December 2008

[4] S. Goel, A. Kumar and M.A. Bayoumi “Design of Robust, Energy-Efficient Full Adders for Deep-Submicrometer Design Using Hybrid-CMOS Logic Style” transactions on Very Large Scale Integration (VLSI) systems, vol. 14, no. 12, december 2006

[5] V. Foroutan, K. Navi and M. Haghparast “A New Low Power Dynamic Full Adder Cell Based on Majority Function” World Applied Sciences Journal 4 (1): 133-141, 2008

[6] Shams, A., Darwish, T., & Bayoumi, M. "Performance analysis of low Power 1-bit CMOS full adder cells". IEEE Trans. Very Large Scale Integr. (VLSI) Syst., 10, (pp. 20-29). (2002)

[7] Chang, C.-H., Gu, J., & Zhang, M. “A review of 0.18um full adder performances for tree structured arithmetic circuits”. Very Large Scale Integration (VLSI) Systems, IEEE Transactions , pp. 686 - 695 (2005).

[8] K. Navi M. Maeen, V. Foroutan, S. Timarchi, O. Kavehei “A novel low-power full-adder cell for low voltage” INTEGRATION, the VLSI journal 42 (2009) 457–467

[9] Alioto, M., & Palumbo, G. "Analysis and comparison on full adder block in submicron technology" IEEE Trans. Very Large Scale (VLSI) Syst., vol. 10, no. 6, (pp. 806–823) (2002).

[10] Navi, K., & Kavehe, O. "A novel low-power full-adder cell for low voltage". INTEGRATION, the VLSI journal 42 , pp. 457 - 467 (2009).

[11] K. Navi, V. Foroutan, M. Rahimi Azghadi, M. Maeen, M. Ebrahimpour, M. Kaveh, O. Kavehei “A novel low-power full-adder cell with new technique in designing logical gates based on static CMOS inverter” Microelectronics Journal 40 (2009) 1441–1448

[12] S. Saravanan, and M. Madheswaran “Modified Multiply and Accumulate Unit with Hybrid Encoded Reduced Transition Activity Technique Equipped Multiplier and Low Power 0.13µm Adder for Image Processing Applications” 2010 International Journal of Computer Applications (0975 – 8887) Volume 1 – No. 9

[13] A. Bazzazi and B. Eskafi “Design and Implementation of Full Adder Cell with the GDI Technique Based on 0.18µm CMOS Technology” Procedings of the International MultiConference of Engineers and Computer Scientists 2010 Vol II, IMECS 2010, March 17-19, 2010, Hong Kong

[14] PTM. (s.d.). Fonte: Predictive Technology Model: http://ptm.asu.edu/