

# Evaluating the Efficacy of Low Power Process to Design Low Power Circuits

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## Abstract

*The power consumption is the major design constraint for portable products. This paper investigates the effect of lowering the supply voltage on the energy and performance efficiency of CMOS circuits designed with different transistor types: low-power and high-performance. It is shown that for the same dynamic power constraint, a high performance design achieve better performance than the low-power one. However, the static power consumption is significantly higher in high-performance process. Nevertheless leakage reduction techniques can be used to avoid this higher static consumption.*

## 1. Introduction

The dimension of the device in VLSI technology has scaled down significantly for the last years. This miniaturization of the devices in each new MOSFET technology generation has provided continual improvements in integrated circuits performance and functionalities, reducing the cost per function.

In the past, only specific markets required low-power integrated circuits. The main goal of designers always was achieve the better performance with acceptable power and area. For the last years, there was an explosive growth in portable systems, like mobile phones, wireless sensor, medical electronics tablets and smartphones. Since the capacity of the batteries of those portable electronic products are limited, the power consumption becomes a very important constrain to the designers, and increases his importance as research area in microelectronics.

The researches propose numerous techniques for achieving low power, on several different levels of abstraction [2-5]. One of the more efficient approaches is design the digital circuits with transistors operated in subthreshold region or near-threshold [3]. In subthreshold designs, the subthreshold current provides a near ideal voltage transfer characteristics of the logic gates. Its impact on system design is an exponential reduction of power at the cost of reduced performance [3].

In micrometer designs, the static current is usually ignored due to its insignificant value when compared to dynamic power. The device dimension scaling increases the electric field between transistor structures increasing the magnitude of this static current [6]. In modern designs, if none leakage reduction technique is applied, the static power can respond for more than 50% of total power consumption [7].

At technology level, two or more types of transistors have been developed to assist designers to reduce the power consumption. The main difference between these types is the threshold voltage ( $V_{th}$ ). In Low Power (LP) process the transistor threshold voltage is higher than in High Performance (HP) process. A transistor with higher threshold voltage has higher subthreshold and saturated current when compared to similar transistor with lower threshold voltage. This reduced current magnitude in LP type will reflect in a higher circuit delay.

The goal of this paper is evaluate the efficacy of these two transistor types to achieve low power consumption with fewer penalties in performance. The analysis verifies the behavior when different values of supply voltage are applied in the circuit.

Section 2 introduces the basic power concepts in CMOS circuits. Section 3 details how the experiments are executed and Section 4 comments the simulation results. Finally conclusions are presented in Section 5.

## 2. Power in CMOS Circuits

The power dissipation in digital CMOS circuits can be decomposed in two parts, which are summarized in the following equation:

$$P_{total} = P_{dynamic} + P_{static} \quad (1)$$

The first term represents the dynamic component of power. This portion is also composed by two parts as presented in equation (2).

$$P_{dynamic} = P_{switching} + P_{short-circuit} \quad (2)$$

The switching power  $P_{switching}$  is due to the charge and discharge of the capacitors driven by the circuit. It is modeled by the following equation:

$$P_{switching} = \frac{1}{2} \cdot C_L \cdot V_{DD}^2 \cdot f \cdot \alpha \quad (3)$$

where  $C_L$  is the output load of the gate,  $V_{DD}$  is the supply voltage,  $f$  is the clock frequency and  $\alpha$  is the switching activity of the gate, defined as the probability of the gate output to make a logic transition during one clock cycle.

The short-circuit power  $P_{short-circuit}$  is caused by the short circuit currents that arise when pairs of PMOS/NMOS transistors are conducting simultaneously in a CMOS gate, this power can be represented for the below equation. It is well explored in [8].

$$P_{short-circuit} = I_{short-circuit} \cdot V_{DD} \quad (4)$$

The second term in equation (1) represents the static power component of total power. It is also called leakage power. It is due to the leakage current that flows in the circuit such as subthreshold, gate tunneling or reverse-biased PN junction leakages for instance [6]. The static power is defined as in the equation:

$$P_{static} = I_{leakage} \cdot V_{DD} \quad (5)$$

For older technologies (0.25 $\mu$ m and above),  $P_{switching}$  was predominant and the static current could be ignored. For nanometer processes,  $P_{static}$  becomes more important and should be considered in the total power dissipation analysis [7].

### 3. Methodology

To evaluate the efficacy of low power process to design low power circuits, this work simulates a set of circuits and compare power and performance results. The circuits are designed with two different types of transistors: a low-power (LP) and a high-performance (HP), the threshold voltage is approximately 0,6V and 0,3V, respectively. All results are obtained using the electrical simulator NGSPICE [9]. Two predictive technology models BSIM4 are used in this analysis: 32nm LP and 32nm HP [10]. The analysis is divided in three experiments: Single inverter, 17-stage Ring Oscillator and the ISCAS 85 C17 benchmark circuit [11].

The adopted strategy to reduce power is the power-driven voltage scaling, reducing supply voltage with transistors operating in the subthreshold region [12]. In all simulations, the Vdd value starts with the nominal value of 1V and is reduced in a voltage step of 0.1V while the logical behavior still correct.

All experiments follow next steps:

1. Describe the circuit with typical Vdd
2. While logical behavior is correct
  - 2.1. Simulate with HP transistor type
  - 2.2. Simulate with LP transistor type
  - 2.3. Extract power and timing values
  - 2.4. Reduce Vdd applied to all circuit (0.1V step down)
3. Compare the results for the 2 transistor types finding the optimal operation point taking into account the power and delay.

### 4. Simulation Results

The possibilities of improve the performance of low power CMOS circuits is explored by reducing the supply voltage in high performance transistor type instead use low power transistor type. The first analysis is performed in the simplest cell, the inverter. Table 1 presents delay, power and current results of inverters designed with both PTM 32nm high-performance (HP) and low-power (LP) transistor type, with  $W_n = 70$ nm and  $W_p = 140$ nm at nominal temperature for several values of power supply.

Figure 1 summarizes the relation between dynamic power and performance of this inverters. In this picture it is clearer that for the same power constraint, a high-performance transistor type achieve better performance than low power transistor type. It is possible since the power supplies values are different. The HP has supply voltage smaller than the LP for the same power constraint. Instead of this smaller supply voltage value, the performance is better in HP process since its threshold voltage is almost half of the threshold voltage of LP process. However, when Ultra-low-power is required, the LP process can reduce by more than two orders of magnitude the power consumption when compared to HP process.

Table 1 – Simulation results for inverter designed in LP and HP process for several power supply voltages

| $V_{dd}$<br>(V) | $I_{peak}$ (uA) |       | $P_{dynamic}$ (uW) |      | Average Delay (ns) |      | $I_{sub}$ (pA) |         | $I_{gate}$ (pA) |       | $I_{BTBT}$ (pA) |      |
|-----------------|-----------------|-------|--------------------|------|--------------------|------|----------------|---------|-----------------|-------|-----------------|------|
|                 | LP              | HP    | LP                 | HP   | LP                 | HP   | LP             | HP      | LP              | HP    | LP              | HP   |
| 1.0             | 6,63            | 15,20 | 1,45               | 4,10 | 0,07               | 0,01 | 3,09           | 5519,64 | 18,38           | 61,07 | 1,01            | 1,00 |
| 0.9             | 4,88            | 8,20  | 0,94               | 2,07 | 0,1                | 0,01 | 2,26           | 2889,67 | 9,23            | 33,10 | 0,91            | 0,90 |
| 0.8             | 3,50            | 4,25  | 0,63               | 0,95 | 0,14               | 0,02 | 1,67           | 1587,27 | 4,06            | 18,88 | 0,81            | 0,80 |
| 0.7             | 2,11            | 2,44  | 0,41               | 0,44 | 0,19               | 0,05 | 1,25           | 903,43  | 1,33            | 10,49 | 0,71            | 0,70 |
| 0.6             | 0,76            | 1,53  | 0,17               | 0,21 | 0,34               | 0,11 | 0,94           | 525,38  | 0,17            | 5,45  | 0,61            | 0,60 |
| 0.5             | 0,01            | 0,91  | 0,02               | 0,1  | 1,98               | 0,23 | 0,70           | 308,84  | ~0,00           | 2,58  | 0,51            | 0,50 |
| 0.4             | 0,01            | 0,31  | ~0,00              | 0,04 | 18,9               | 0,44 | 0,53           | 182,45  | ~0,00           | 1,24  | 0,41            | 0,40 |
| 0.3             | ~0,00           | 0,05  | ~0,00              | 0,01 | 201                | 1,79 | 0,39           | 107,96  | ~0,00           | 0,55  | 0,30            | 0,30 |

Since the static current is also an issue in nanometer technologies, Figure 2 shows the inverter static current for several values of power supply for both evaluated process. The LP transistor type has significant reduction in subthreshold current since its threshold voltage is higher than HP transistor type. Figure 3 shows that in LP transistor the subthreshold current is reduced below the gate leakage current.

The second and third experiment consist in evaluates the power and performance behavior of a ring oscillator and a benchmark circuit design in both LP and HP transistor type for several supply voltage values. As illustrated in Figures 4, 5, 6, and 7, the same behavior verified in inverter analysis is obtained.

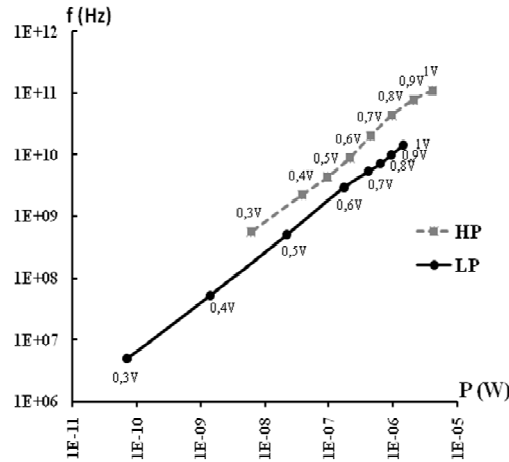


Fig. 1 – Operation frequency versus Dynamic Power of an inverter designed in LP and HP transistor type for supply voltage from 1V to 0.3V

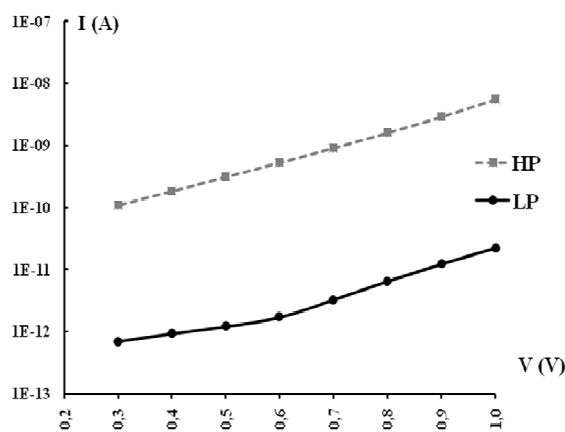


Fig. 2 – Static current in inverters designed in LP and HP transistor type for several values of power supply

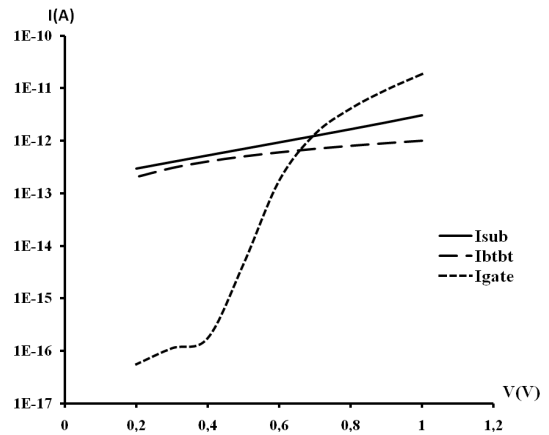


Fig. 3 – Static current components of the inverter designed with LP transistor for several supply values

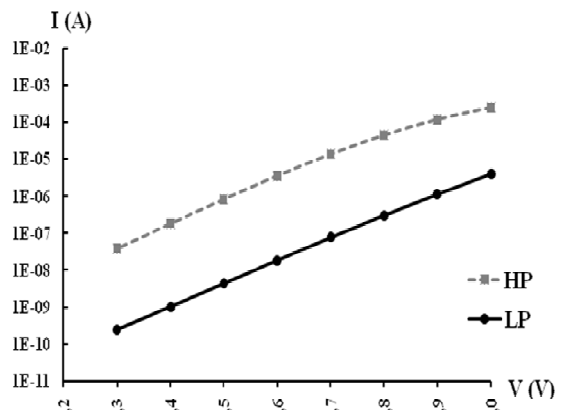
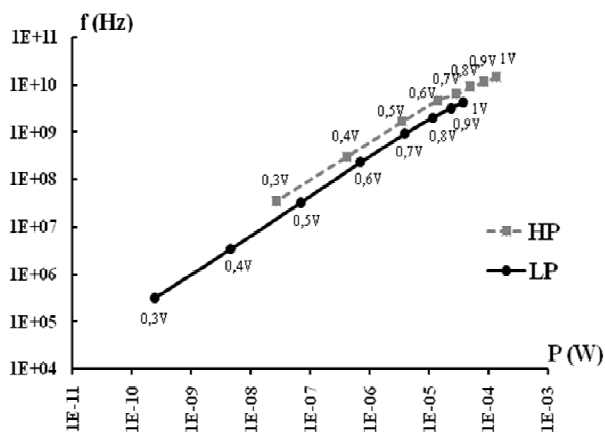


Fig. 4 – Operation frequency versus power of a 17-stage ring oscillator designed in LP and HP process for supply voltage from 1V to 0.3V

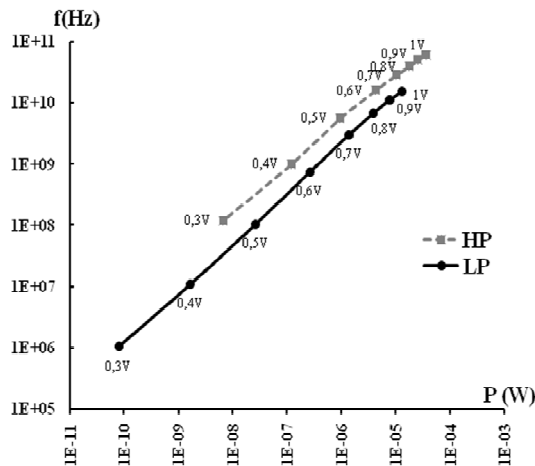


Fig. 6 – Operation frequency versus power of the C17 benchmark circuit designed in LP and HP transistor type for supply voltage from 1V to 0.3V

Fig. 5 – Static current in a 17-stage ring oscillator designed in LP and HP transistor type for several values of power supply

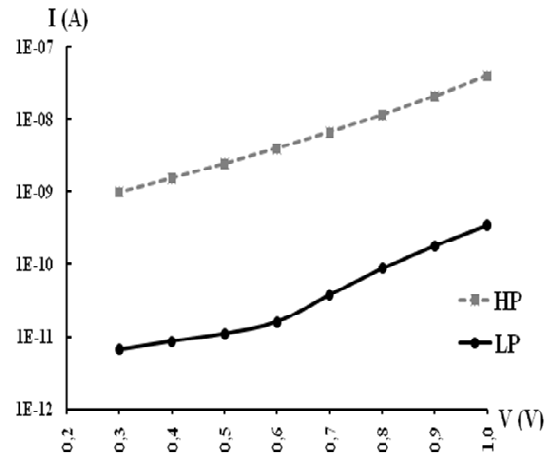


Fig. 7 – Static current in the C17 benchmark circuit designed in LP and HP transistor type for several values of power supply

## 5. Conclusions and Final Remarks

This work has investigated the tradeoffs of reducing the power consumption of CMOS systems when two transistor types, low-power (LP) and high-performance (HP) are available in the technology process. The power reduction was obtained by reducing the supply voltage. The investigation has been done by electrical simulations of several circuits, verifying their proper function and getting their performance and power consumption values. The results show that LP design has minimum power consumption (ultra-low-power) that is not achieved by HP. However, for a wide range of power consumption, the HP design achieves a better performance result for the same power constraint.

## 6. References

- [1] G. E. Moore, "Cramming More Components onto Integrated Circuits," *Electronics*, April 19, 1965, pp. 114–117.
- [2] A. P. Chandrakasan, S. Sheng, and R. W. Brodersen, "Low-power CMOS digital design," *IEEE Journal of Solid-State Circuits*, vol. 27, no. 4, pp. 473–484, 1992.
- [3] R. Vaddi, S. Dasgupta and R. P. Agarwal, "Device and Circuit Design Challenges in the Digital Subthreshold Region for Ultralow-Power Application", *VLSI Design*, 2009.
- [4] R. Gonzalez, B. M. Gordon and M. Horowitz, "Supply and Threshold Voltage Scaling for Low Power CMOS", *IEEE Journal of Solid-State Circuits*, vol. 32, no.8, Aug. 1997, pp.1210 - 1216
- [5] M. Qazi, M. E. Sinangil and A. P. Chandrakasan, "Challenges and Directions for Low-Voltage SRAM", *IEEE Design and Test of Computers*, vol. 28 no.1, 2011, pp.32 – 43.
- [6] ROY, K. et al. "Leakage Current Mechanisms and Leakage Reduction Techniques in Deep-Submicrometer CMOS Circuits," *Proceedings of IEEE*, vol. 91, no. 2, Feb. 2003, pp. 302-327.
- [7] International Technology Roadmap for Semiconductors, 2007 Edition. Available at <http://public.itrs.net>
- [8] Veendrick, H. J. M., "Short-circuit dissipation of static CMOS circuitry and its impact on the design of buffer circuits," *Journal of Solid-State Circuits*, vol. 19, no. 4, pp. 468–473, Aug. 1984.
- [9] P. Nenzi and H. Vogt. *NGSPICE Users Manual Version 22*, 2010. available at <http://ngspice.sourceforge.net/>
- [10] W. Zhao, Y. Cao, "New generation of Predictive Technology Model for sub-45nm early design exploration," *IEEE Transactions on Electron Devices*, vol. 53, no. 11, pp. 2816-2823, November 2006.
- [11] David Bryan, "ISCAS'85 Benchmark Circuits and Netlist Format", North Carolina State University
- [12] A. Chandrakasan and R. Brodersen, *Low-Power CMOS Design*. IEEE Press, 1998.