Architectural Design for the Adaptive Loop Filter of the Emerging High Efficiency Video Coding Standard

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Abstract

This work presents the design and synthesis of an architecture for the Adaptive Loop Filter (ALF), one of the three filters that compose the In-Loop Filter of the emerging High Efficiency Video Coding (HEVC) standard. The architecture was described in VHDL and synthesized to an Altera Stratix I FPGA. The ALF is not applied to all coding unities, but only to that ones that are marked as ON for filtering and this definition is done by the global encoder control. Considering the worst case, when all the samples in the frame are filtered, the designed architecture is able to process SDTV frames in real time reaching 118 frames per second.

1. Introduction

On January 2010, the Joint Collaborative Team on Video Coding (JCT-VC) was created as a group of video coding experts from ITU-T and ISO/IEC intending to create a new and most efficient video coding standard. Proposals were evaluated using a software called Test Model under Consideration (TMuC). The emerging standard was officially named as High Efficiency Video Coding (HEVC) [1] and its first software version available for test was named HEVC Model (HM) [2] which is considered the golden model for our hardware design. The initial objective of the HEVC was to provide the double of the compression rates with the same or reduced computational complexity when compared to the current state-of-the-art H.264/AVC [3] standard. To achieve this objective was necessary to incorporate new tools and techniques which did not exist in previous standards.

The coding process aims to reduce many types of redundancy presented in digital videos. During this processing, the subjective quality can be deteriorated, especially through the quantization step which inserts artifacts in the video as a collateral effect to increase the compression rate. Recently, new filters are being considered inside encoders and proposed to scientific community. HEVC proposed set of three filters called In-Loop Filter which contains traditional Deblocking Filter (DF) besides bringing the new Sample Adaptive Offset (SAO) and Adaptive Loop Filter (ALF). The HEVC coder has two configurations sets, the High Efficiency (HE) and the Low Complexity (LC) [2]. The ALF is only supported by the High Efficiency configuration, and DF and SAO are supported by both configurations.

The ALF, focus of this work, is an innovation proposed by HEVC and it works to reduce an additional distortion error generated in all previous coding steps.

This work presents a hardware implementation focusing on the most used configuration of Adaptive Loop Filter: the filter with a 5x5 core size. This filter is used in the decision process to define which frame region will or not will be filtered and it is also used in the full filtering process. The solution presented in this paper aims to improve the order of operations done in the filter.

2. HEVC Adaptive Loop Filter

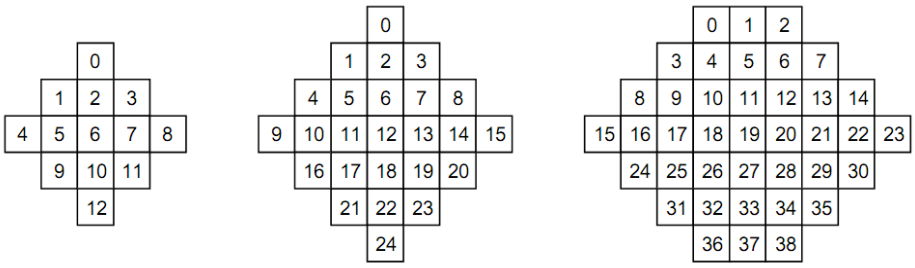
The goal of this work is to design hardware solutions for the In-Loop Filter defined by the new standard HEVC. The In-Loop filter is used to reduce the distortions introduced by the quantization step and then it improves the subjective image quality. The In-Loop Filter proposed for the HEVC is composed by the Deblocking Filter (DF), followed by the Sample Adaptive Offset (SAO) and finally by the Adaptive Loop Filter (ALF).

The DF is applied to the block edges and it improves the distortion and the subjective image quality. This filter is similar to that defined in the H.264/AVC standard. The SAO is applied after the DF and it considers the local properties of the image, like the edge of objects. In this filter, there are two offset types: the band offset and the edge offset. The SAO is an innovation introduced by HEVC.

The third filter in the In-Loop Filter is ALF, which is explored on this work. The ALF is a tool proposed by the JCT-VC that aims to reduce the distortion in relation to the original image. This filter is applied to the reconstructed image after the DF and SAO applications. ALF is another innovation proposed by HEVC and it works to reduce an additional distortion error generated in all previous coding steps, especially at the quantization step. This filter uses a diamond shape of three sizes: 5x5, 7x7 and 9x9 pixels. The filter

coefficients are statically defined by the Wiener Filter that generates the coefficients accordingly to the historical contribution of the filtering process, which is influenced by the image characteristics.

The ALF filtering process for luminance samples uses multiple diamond shaped 2-D filters and the filter coefficients for each pixel are selected from multiple filters by the variance evaluation. There are three allowed filter sizes: 5x5, 7x7 and 9x9, but the maximum vertical difference for the current pixel is restricted from -3 to 3, as shown in fig. 1.



(a) alfTap = 5 (a) alfTap = 7 (a) alfTap = 9

Fig. 1. Filter shapes for luminance samples [4]

Many alternatives for the ALF implementation were proposed in the JCT-VC meetings. Two of them were suggested on March, 2011, in Geneva. O ne uses a block level ALF [5] and another one proposed an adaption between the block based version and a region based version [6].

There are also two algorithms to apply the filter. One of them was the originally presented in the first HM software, and it is a 16-pass algorithm; and the other one is called one-pass algorithm [7]. The one-pass algorithm is now included also in the HM software and it can be used setting a variable in the configuration file of the encoding process.

The ALF filter application is done at the Coding Unit (CU) level, where the filter is applied pixel by pixel in the slice. In order to apply the ALF, firstly the encoder must decide which regions of the frame must be filtered. To decide which regions will be or not filtered, in the 16-pass algorithm, a simplified filter (5x5) is applied in all regions. Then the distortion obtained is compared with the distortion without filter application. The regions where the distortion was improved are marked as ON, and regions with worst results are marked as OFF. The full filtering process applies three sizes of filters and compares the results to find the best filter to be used. This stage is done only for regions marked as ON. The main difference inserted by the one-pass algorithm is that the 5x5 ALF filter does not need to be applied for all frame to decide the ON and OFF regions, the decision is derived from previously encoded frames, because it considers the similarity among neighbor frames.

Considering hardware implementations, only one work was found in the literature. An architecture was proposed for one type of ALF filter in Du and Yu [8]. However, this implementation is still focused in the H.264/AVC standard, and it uses square filters shapes and the proposed architecture was developed together with the DF. We did not find in the literature any published implementation focusing on the HEVC ALF.

3. Proposed Architecture

This paper proposes a hardware implementation of the HEVC ALF filter. This design is based in the decisions of the JCT-VC meeting realized in Geneva on March, 2011. Then, the hardware design is based on the Working Draft 3 [4] and the Test Model HM3 [9].

Based on the Working Draft 3, three sub-processes were identified in the whole ALF filtering process. The first sub-process is the boundary padding and it is necessary in the filter process because the processing is done at a coding unit level. If the coding unit border does not coincide with the slice border, the border will be pad with neighboring samples, but if the coding unit border coincides with a slice border, the pad will be done with a copy of the coding unit border samples.

The next sub-process after the boundary padding is the filter coefficients derivation. The investigation of this step was not concluded in this work.

The last sub-process is the filter process itself. Fig. 2 presents two sets of values for the filter with a 5x5 shape. Fig. 2 (a) illustrates the image samples that will be used in the filtering process to generate the new value for the sample “g”. Moreover in fig. 2 (b) shows the coefficients that will be used in the process.

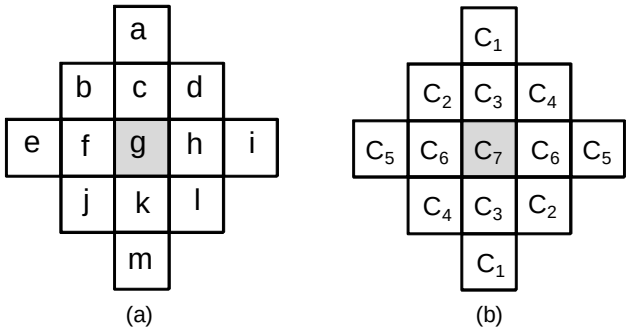


Fig. 2. ALF filter with a 5x5 shape.

The filter process corresponds to a multiplication of the sample with its corresponding coefficient and the sum of these partial multiplications. Considering that the filter coefficients are symmetrically distributed, it is possible to reduce the number of multipliers. Instead of multiplying each sample by the correspondent coefficient, it is possible first add the samples that will be multiplied by the same coefficient and after realize the multiplication. This process will reduce the number of multipliers from 13 to 7. This calculation order was already proposed by the HM software.

The architecture designed in this work is shown in fig. 3. This figure shows the adders grouping the samples that will be multiplied by the same coefficient and, in sequence, the multipliers. The clipping sum was dislocated to be done in parallel with other adders.

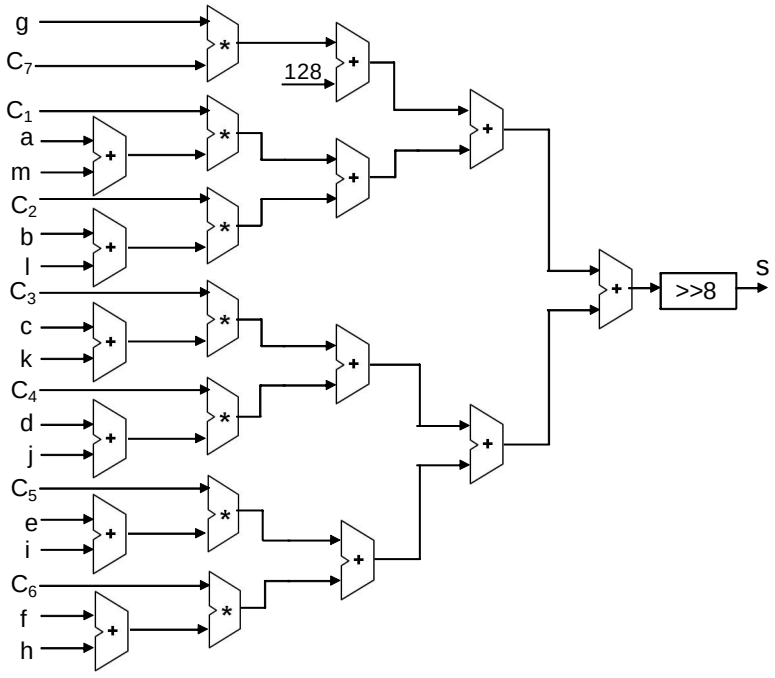


Fig. 3. Designed architecture for 5x5 ALF core.

The architecture was described in VHDL and synthesized targeting Altera FPGA Stratix I EP1S10F484C5 using the Quartus II tool.

4. Results and Discussion

Tab.1 presents the synthesis results for the 5x5 ALF core. With the period reached in the synthesis process, the processing rate was estimated. Considering SDTV resolution (720x480 pixels) the architecture can process 107 frames per second and for Full HD resolution (1920x1080 pixels) it can process 19.6 frames per second, both in the worst case.

Tab. 1. Synthesis results for the proposed architecture for ALF 5x5 core.

	Used Resources
Logical Elements	113
DSP 9 bits	13
Period	≈ 24.5 ns
Synthesis targeting Stratix I EP1S10F484C5 device	

These results show that the designed architecture is able to process SDTV frames in real time (30 frames per second), but it can not process Full HD frames in real time. These results are function of the fully combinational strategy used in this design, where four adders and one multiplier are serially connected. This solution uses a lower amount of hardware resources at a cost of a reduced processing rate. Moreover, the processing rate estimative considers that all CUs are filtered, which does not occur frequently.

The work of Du and Yu [8] presents a hardware implementation of an ALF filter, however, it has a different approach from that the used in our work, which prevents a fair comparison. The proposal of Du and Yu [8] focused on H.264/AVC, and uses a different filter shape and proposes an architecture combined with the DF. The cited work reached an operation frequency of 211MHz (when targeting a Xilinx Virtex 5 FPGA), achieving real time processing for Full HD videos. The number of operators used in the 9x9 filter proposed by Du and Yu [8] was of 41 multipliers and 81 adders, while in an architecture for the same filter and using a similar strategy than that used in our work for a 9x9 shape, only 20 multipliers and 39 adders would be used. However, there is a difference in the used shape between the two filter versions, which makes a direct comparison unfair.

5. Conclusions

In this work an investigation about the HEVC ALF filter was presented. ALF is one filter of the In-Loop Filter proposed by the new HEVC standard . This paper also presented the hardware design of the 5x5 ALF filter core that was described in VHDL and synthesized for an Altera FPGA.

The synthesis results show that the designed architecture is able to process 118 SDTV frames per second, achieving real time processing. However, for Full HD resolution, the architecture achieved only 19.6 frames per second. But it is important to notice that the used evaluation considered the worst case, where all samples inside a frame will be processed by the ALF.

As future work it is planned to continue the investigation of the Working Draft and HM in order to identify the stages that were not fully investigated in this work, thus targeting to obtain a complete architecture for the ALF. Another future work is to look for alternatives to optimize the filter architecture core to achieve higher processing rates and also trying to reduce hardware use and power consumption.

6. References

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