Logic Gates Design for Aging Enhancement

[1,2]Paulo F. Butzen, [2]Vinícius Dal Bem, [2]André I. Reis, [2]Renato P. Ribas
paulobutzen@furg.br, {vdbem, andreis, rpribas}@inf.ufrgs.br

[1]Centro de Ciências Computacionais - Universidade Federal do Rio Grande - FURG
[2] PGMICRO – Universidade Federal do Rio Grande do Sul

Abstract

The continuous scaling in transistor dimensions turns device reliability one of the major concern for nanometer design. This work aims to evaluate the effects of three aging mechanisms in the reliability of different logic gate designs. Electrical simulations associated to analytical and spice wearout models are used to compute the circuit degradation. Simulation results reveal that the restructuring of intra-cell transistor networks recovers up to 17% of delay impact, while the decomposition of single stage circuits into multi-stage topologies tends to produce worst results in terms of performance variability.

1. Introduction

CMOS technology has been permanently scaling down during the last decades. Several aspects ignored in earlier technology nodes are becoming critical concerns in nanoscaled design [1-3]. The circuit reliability is one of the major challenges in nanometer CMOS circuits [4]. Aging mechanisms, such as Hot Carrier Effect (HCE), Negative-Bias Temperature Instability (NBTI), and Time-Dependent Dielectric Breakdown (TDDB) become a serious issue to guarantee the circuit reliability during entire system lifetime.

Thus, in order to obtain the overall circuit constraints, the reliability must be modeled and analyzed since at very beginning of design stage. In this sense, logic functions can be designed using different transistor networks. These variations can be achieved by using different logic styles or by restructuring the transistor arrangements. Also, such logic functions can be decomposed into multiple stages. These different topologies tend to present different levels of degradation due to wearout mechanisms [6].

In order to achieve a robust design, many solutions to mitigate wearout degradation have been proposed in the literature [3,5,7-9]. At circuit level, some techniques explore the input signal dependence by reordering the gate inputs [7]. Others insert additional modules to explore supply and threshold voltage dependence [8]. At gate level, there are techniques that add a time slack margin to compensate the degradation upsizing the transistors width [3]. Most of proposed techniques deal with only one wearout mechanism. The interaction of different mechanism may produce a worst scenario [9].

In this paper, a methodology to evaluate and quantify the long term aging effect in CMOS logic gates is explored. The method explores the signal and switching probability of different transistor arrangement. From this procedure, some guidelines to design robust gates are presented considering the aging effects individually and their interaction. The design of CMOS gates considering multiple stages is also evaluated.

2. Aging Mechanisms

The shrinking in critical transistor dimensions to nanometer ranges and the increasing doping densities result in a significant increase of electric fields in the channel region of MOS transistors. These high electric fields act in several ways changing the transistor characteristics during its lifetime, as reported in following.

2.1. NBTI

Negative Bias Temperature Instability (NBTI) refers to the generation of positive oxide charge and interface traps in metal-oxide-silicon structure under negative gate voltage bias ($V_{gs} = -V_{dd}$), in particular at elevated temperature [7]. This effect degrades more the PMOS than the NMOS transistors. It increases the PMOS transistor threshold voltage (V_{th}) over time, reducing the device drive current and circuit speed [8]. For a specific technology node and a given set of environmental conditions, the ΔV_{th_NBTI} can be expressed by equation (1) as a function of the transistor stress probability (TSP) [10].

$$\Delta V_{th\_NBTI} = a \cdot (TSP \cdot t)^n \quad (1)$$

where ‘a’ is a technology dependent constant, ‘t’ is the time, and ‘n’ is the NBTI time exponential constant.

The TSP is the probability that PMOS transistor is negative biasing. It is a function of input signal probability and the position of the transistor in the arrangement [6].

2.2. HCE

Hot Carrier Effect (HCE) consists in the process where some electrons and holes that are travelling in the channel and gain enough kinetic energy to be injected into the gate oxide and cause permanent changes in the

oxide-interface charge distribution [11]. This process also results in a shift in the transistor threshold voltage. Due to the fact that the mobility of the electrons is higher than the holes, the NMOS transistors are more degraded than PMOS transistors [12]. For a specific technology node and for a given set of environmental conditions, the ΔV_{th_HCE} can be expressed by equation (2) as a function of the transistor switching HCE degradation probability (TSwP) [12].

$$\Delta V_{th\_HCE} = b \cdot (TSwP \cdot t)^m \quad (2)$$

where 'b' is a technology dependent constant, 't' is the time, and 'm' is the HCE time exponential constant.

The TSwP is the probability when the transistor suffers HCE degradation. It depends on the transistor switching probability and its position in the transistor arrangement.

2.3. TDDB

Time Dependent Dielectric Breakdown (TDDB) can be defined as the process when a conducting path appears between the gate and the channel [13]. This conducting path is caused by the large electric field in the gate oxide that eventually forms traps in the oxide. Once enough traps are formed, they start affecting the device gate tunneling current [14]. A power law is usually applied to model the TBBD degradation [13]. In this work, the power law model is converted to a dependent resistance model as described in equation (3)

$$R_{gd} = K \cdot (TSP \cdot t)^p \quad (3)$$

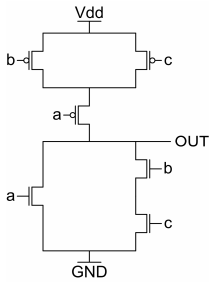
where 'K' and 'p' are technology dependent constants, 't' is the time, 'TSP' is the transistor stress probability. Since TDDB degrades both PMOS and NMOS transistors, the TSP is the probability that PMOS is negative biasing, or the probability that NMOS is positive biasing.

2.4. Interation between mechanisms

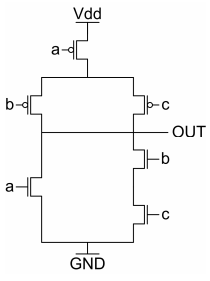
Each of the previous mechanisms has its own particularities, but their effects in devices should be combined to provide a more accurate estimation of total wearout degradation. This interaction may provide opposite results when compared to techniques that evaluate the mechanisms individually [9].

3. Transistor Arrangements and Probability

Several logic functions can be designed using different transistor networks [5]. As mentioned before, these variations can be achieved by using different logic styles, by restructuring the transistor arrangements, and by decomposing the logic function in more than one stage. For instance, Fig. 1 shows two versions of traditional CMOS AOI21 gate with restructured PMOS pull-up plane. Fig. 2 shows the logic function "OUT = a·c + a·c·e + e·c·d + b·e" designed over conventional CMOS topology and using bridge concept. Also, the logic functions can be decomposed into multiple stages, as the NAND3 gate depicted in Fig. 3.

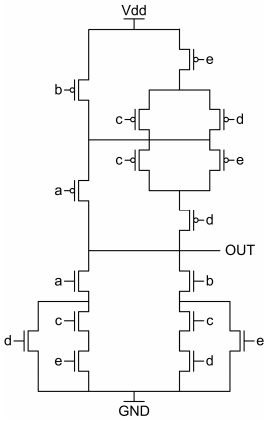


(a)

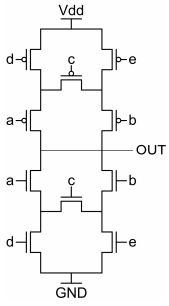


(b)

Fig. 1. Two logically equivalent AOI21 CMOS gates.

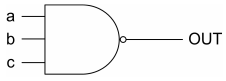


(a)

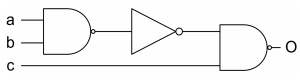


(b)

Fig. 2. Logic gate "OUT = a·c + a·c·e + e·c·d + b·e": (a) conventional CMOS (b) 'bridge' topology



(a)



(b)

Fig. 3. NAND3: (a) single gate and (b) multi-stage circuit.

The concepts of transistor stress probability (TSP) and transistor switching HCE degradation probability (TSwP) can be considered the first step to compute the device degradation in the transistor arrangement.

The TSP has been previously defined as the probability that PMOS is negative biasing or the probability that NMOS is positive biasing. The TSP is a function of input signal probability and the position of the transistor in the network arrangement. In previous work [10], only the input signal probability has been

considered to define the transistor stress condition. However, when transistor stacks are present in the arrangement, the position of the device has to be taken into account in the evaluation of stress probabilities [6].

The TSwP is the probability that a transistor suffers HCE degradation. Since the HCE effect is exponentially dependent of V_{ds} [12], only transistors that are directly connected to the output suffer significant HCE degradation. For this reason, the switching activity is not enough to compute the degradation due to such effect. The transistor position in the arrangement has to be considered for a more accurate evaluation.

4. Aging Robustness Logic Gate Design Guidelines

The following guidelines explore particularities of each mechanism individually. Cases where different mechanisms present the same characteristic are mentioned.

Several considerations could be pointed out when the transistor stack is explored.

- To prevent NBTI and TDDB degradation, the transistors with higher ON probability (input '1' for NMOS and '0'for PMOS) should be placed far from power supplies. This has been already reported considering only NBTI [7].
- From the same reason, when the transistor arrangement is a combination of series/parallel structures, both NBTI and TDDB degradation can be mitigated placing as many transistor as possible close to the output node. This concept has also been already reported considering only NBTI [6].
- To mitigate HCE degradation, both previous statements are opposite. As the HCE effect is exponentially dependent of Vds, the transistor with higher switching probability should be placed close to the power supply. Also, the amount of transistors far from the output node should be maximized.

Assuming that NBTI affects mainly PMOS transistors and HCE mainly NMOS transistor, the above remarks to deal with NBTI and HCE can be applied together at same gate. The complementarity of HCE and TDDB in pull-down NMOS plane let the designer to choose the proper guideline to be followed according to the severity of the effects. From previous statement, the logic planes that present transistor stacks should be more robust against aging effect than the planes that have only single devices between the power supply and the output node.

The following consideration is related to the choice between designing a logic function in one complex single stage or using several simple gates to implement the function in a multiple-stages version.

- Designing a logic function in more than one stage could use a higher number of transistors, increasing the number of devices under degradation. Also, the intrinsic stack robustness is mitigated due to the simple structures, reducing the aging robustness.

5. Simulation Results

The long terms models presented in Section 2 are used to estimate the device degradation due to aging effects over 10 years. As the severity of aging mechanisms depends on the technology under evaluation, the degradation applied in this work considered a maximum V_{th} impact of 50 mV for NBTI and HCE effects, and a range of breakdown resistance from GΩ (fresh device) to KΩ (maximum degraded device) for TDDB effect. The behaviour of each mechanism follows the models reported in the literature [7- 14].

The predictive 32 nm CMOS process has been used to describe the circuits [15]. The stress probabilities for the devices have been computed considering the specific position of each device in the transistor arrangement, equal switching activity and signal probability of 0.5 for all inputs. In functions designed in multi stages, the probability of the logic gates were used to compute the stress probabilities. Electrical characterization has been executed for different design versions of logic functions, considering fanout 4 delay (nominal and degraded).

Table 1 presents the normalized average propagation delay of inverter and NAND2 gates. The columns show the normalized fresh and degraded average delay when NBTI and HCE are considered individually and combined. The results show that the stack transistor recovers 61% of delay degradation due to aging effects.

Table 1 - Average delay degradation in inverter and NAND gates.

		NBTI Degradation (%)	HCI Degradation (%)	Degradation considering effects in-teraction (%)
INV	Tp_HL	-0.18	**8.03**	**7.85**
	Tp_LH	13.87	-0.06	13.83
NAND	Tp_HL	-0.13	**3.23**	**3.08**
	Tp_LH	14.05	-0.23	13.79

The degradation recovered due to transistor arrangement restructuring, illustrated in Fig. 1, is presented in Table 2. The results from both NAND3 design, illustrated in Fig. 3, is also presented in Table 2. The restructuring shows a recovery of 17%, while the use of only one complex single stage achieves savings in order of 27% when compared to multiple stages design.

Table 3 shows the normalized leakage degradation due to TDDB effect in the gates depicted in Fig. 1 and in Fig. 3. The higher degradation verified in the multiple stage NAND3 is due to the use of simple structures that usually have higher leakage per transistor and suffer higher degradation over time.

Table 2 - Average delay degradation in gates depicted in Fig. 1 and in Fig. 3.

Gate	Normalized Average Delay Degradation (%)			Degradation Recovered (%)
	NBTI	HCE	Interaction	
Fig.1(a)	8,26	2,34	**9,80**	**17**
Fig.1(b)	6,63	1,77	**8,38**	
Fig.3(a)	7,09	0,74	**7,63**	**27**
Fig.3(b)	7,40	2,21	**9,71**	

Table 3 - Average leakage degradation due to TDDB in gates depicted in Fig. 1 and in Fig. 3.

Gate	Normalized Average Leakage Degradation due to TDDB effect
Fig.1(a)	2,8 X
Fig.1(b)	2,6 X
Fig.3(a)	3,0 X
Fig.3(b)	6,3 X

6. Conclusions

Different design solutions, that can be used to represent alternative implementations of a certain logic function, have to be explored considering the influence of aging effects in terms of circuit reliability. Electrical simulation results show that the transistor arrangement restructuring is a potential design solution to recover the delay degradation. The use of logic functions designed in one single complex stage instead of multiple stages of simple gates can also be a solution to reduce the aging degradation. To achieve improved reliable design, the guidelines proposed in this work can be easily used together with other techniques already presented in the literature.

7. Acknowledgment

Research partially funded by Nangate Inc. under a Nangate/UFRGS research agreement, by CAPES and CNPq Brazilian funding agencies, by FAPERGS under grant 11/2053-9 (Pronem)., and by the European Community's Seventh Framework Programme under grant 248538 – Synaptic.

8. References

[1] B.H. Calhoun et al. “Digital Circuit Design Challenges and Opportunities in the Era of Nanoscale CMOS”. Proceedings of IEEE, vol. 96, no. 2, Feb 2008, pp. 343-365

[2] Roy, K. et al., “Leakage Current Mechanisms and Leakage Reduction Techniques in Deep-Submicrometer CMOS Circuits”. Proc. IEEE, vol.91, no.2, Feb 2003, pp. 305-327

[3] Borak “Designing reliable systems from unreliable components: the challenges of transistor variability and degradation”. vol. 25 , no. 6, Nov 2005, pp. 10-16

[4] Shekhar Borkar, et al. “Design and Reliability Challenges in Nanometer Technologies”. DAC 2004

[5] Da Rosa Jr, L. S. et. al. “Switch Level Optimization of Digital CMOS Gate Networks”. ISQED 2009

[6] Butzen, P. F, et al.. “Transistor network restructuring against NBTI degradation”. Microelectronics Reliability, Vol. 50, No. 9-11, Sep-Nov 2010, pp. 1298-1303

[7] Y. Wang et al. “Temperature-Aware NBTI Modeling and the Impact of Input Vector Control on Performance Degradation”. DATE 2007

[8] B. C. Paul et al. “Temporal Performance Degradation under NBTI: Estimation and Design for Improved Reliability of Nanoscale Circuits”. DATE 2006

[9] Li, X., et al. “Compact Modeling of MOSFET Wearout Mechanisms for Circuit-Reliability Simulation”, IEEE TDMR, Vol. 8. No. 8, March 2008, pp. 98 – 121

[10] Wang, W. et al. “An Efficient Method to Identify Critical Gates under Circuit Aging”. ICCAD 2007

[11] Quader, K.N., et al. “Hot-Carrier-Reliability Design Guidelines for CMOS Logic Circuits”, Journal of Solid State Circuits, Vol. 29, No. 3, March 1994, pp. 253-262

[12] Magnone, P., et al. “Impact of Hot Carriers on nMOSFET Variability in 45 and 65 nm CMOS Technologies”, IEEE TED, vol. 58, no. 8, Aug 2011, pp 2347-2353

[13] Kaczer, B., et al. “Impact of MOSFET oxide breakdown on digital circuit operation and reliability”, IEDM 2000

[14] Choudhury, M., et al. “Analytical model for TDDB based performance degradation in combinational logic”, DATE 2010

[15] Zhao, W., Cao, Y. "New generation of Predictive Technology Model for sub-45nm early design exploration," IEEE TED, vol. 53, no. 11, Nov 2006, pp. 2816-2823