A brief analysis of using Transistor Networks

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Abstract

With the evolution of mobile devices, power became a key point in electronic development, and its optimization is a crucial point for the advance of portable device development. A huge amount of techniques had been used along the years, and a great improvement is verified in respect with power, however, according ITRS it's not still enough. Too much need to be done still achieve the target for power in portable devices, but this goal can't be achieve without reach a deep optimization in all levels of abstraction on design development. Using standard cells are easier, fast and reliable, but can't achieve high optimization in physical level design. Why don't use transistor networks? This paper presents an analysis of using transistor networks to build systems, and what are the advantages and disadvantages of its use in newest technologies, compared with using standard cells.

1. Overview

Along the last decades, technology evolution in server/personal computer was very fast, the use of this kind of device became extremely important, being used for different purposes, in many areas. The evolutionary growth of these devices was motivated mainly for need in performance, what means, to process as much as possible information in less amount of time. Taking in mind this goal, hardware designers developed many techniques, and methods looking for performance. Along the years, solutions became devices faster and smaller, making possible integrate a huge number of devices, in the same area used before. With smaller components, came smaller systems, creating a mark point in technology evolution, the mobile generation.

This new generation became projects much more complex, once there is a limited amount of power storage in the portable device; power became a key point in electronic development. Actually, It is a big challenge to reduce the amount of energy consumed in mobile devices keeping the same performance. Many techniques reduce substantially power consumption; however the most efficient imposes limits in processing time. According ITRS 2011 (Figure 1), there was important improvement in power factor in the last years. However, to active the goal expected for the future, too much still need to be done, and the fact is that all development abstraction levels need to be optimized, in order to active this target.

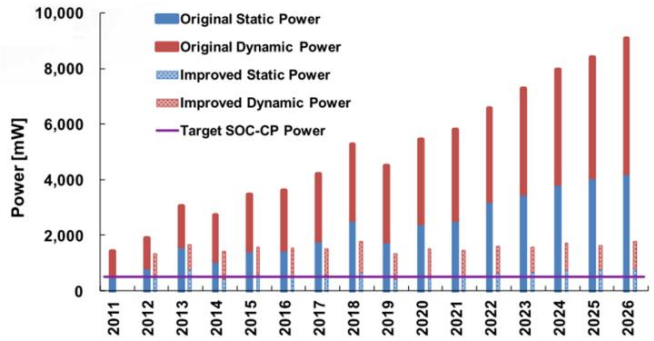

Figure 1: Impact of Low-Power Design Technology on SOC consumer Portable Power Consumption (ITRS Design ITWG 2011).

2. Historical Aspects

For a long time, circuit development was made just by hand. For each component/system a set of mask were drawn and verified, building the whole layout of the design. This approach was done for a couple of years, till development of first tools capable of drawing the layout in computer. Since that generation, too many improvements were done in semiconductor and tool development area. Along the years, companies realized that many projects were done by parts of others projects. Aiming reduces the development time, they started to save his pre-designed projects, and reuse then in future projects, this approach start to create the firsts libraries. Since 90 century, some companies started to create even smaller circuits, called cells. The use of these cells defined a

methodology called standard cells, and is widely use till today. The use of cells became extremely widespread because make easier to build complex system, and there is a high feasibility and reliability. However, even using standard cells methodology, many companies still need to make by hand some parts of the circuit. The motivation for this heterogeneous approach is that in many systems, for instance, in processors; time constraints in critical paths are not reaching just using standard cell methodology.

3. Transistor Networks

Despite standard cells had been widely used for design digital systems, its methodology is quite limited in relationship with optimization. In a traditional standard cell library, the number of cell is limited in a set of about 200 different functions; however, the possible number of logical functions that can be necessary in a synthesis process is much more than this. For sure these cells are enough to descript any circuit; however, lots of circuits won't be optimized. Once synthesizer will need to use an assembling of cells to describe a determine function, represent this same function with just one macro-cell is much less power hungry than using the assembled one.

The study of using transistor networks in new designs is basically a back for old researches, getting the better solutions for full-custom designs in accordance with the newest algorithm and tools technologies, trying to create an automatic manner of building reliable circuits in a comprehensive time.

Traditional synthesis process uses sets of BDD (Binary Decision Diagram) or RBDD (Reduced ordered Binary Decision Diagram), as illustrated in Figure 2, to represent logical functions, and from this, map pre-existents cells in a way that constraints are reached. In a transistor network approach, the process is quite similar; however, instead of mapping pre-designed cells, all the necessary subset of BDDs are created on-the-fly, trying to minimize determined constraints. With this subset defined, designer can use automatic layout generators to create the layout that represent those BDDs, and use commercial simulators to characterize it and continue the traditional place-and-route flow.

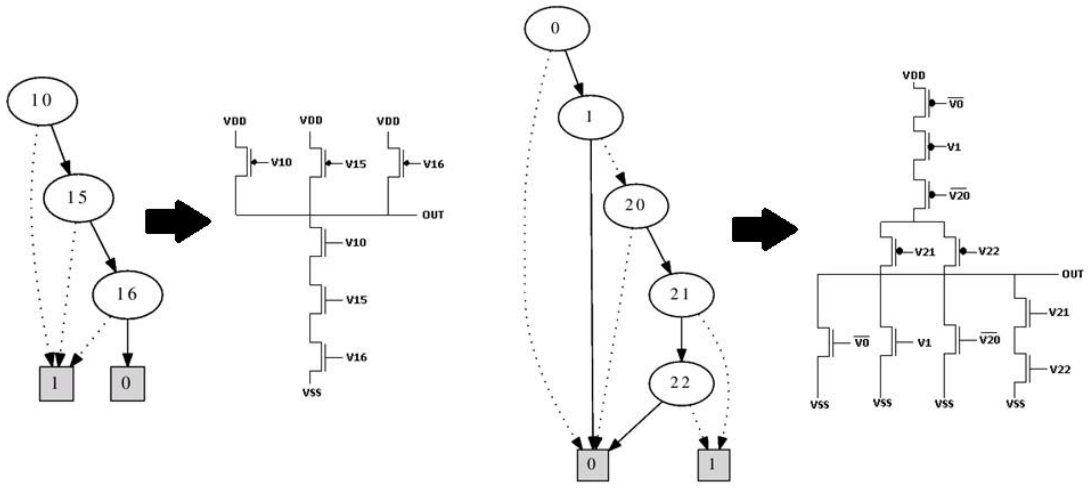

Figure 2: Example of a subset of RBDDs and aside its representation as a transistor network.

4. Benefits and Drawbacks

Using transistor networks makes optimization much more flexible. Once any logical function can be generated according necessity, and the circuits may be sized according pre-defined constraints, optimization process can reach deep improvement in power and timing. In Figure 3 is presented an straightforward example of optimization; In this example a couple of cells are replaced for a single one representing the same logical function. This process are very intuitive, however it is not efficient when using standard cells. The reason was explained in previews session, but with a limited set of cells this replacement, in some cases, are not possible, becoming impossible a deep optimization. In a transistor network approach this problem don't exist, once cells are build on-the-fly, according necessity. The same process occurs when working with fast paths. In traditional standard cell approach, buffer and repeater are commonly inserted to force signal level and ensure that signal reach timing constraints. Using transistor networks, sizing can be done as close as possible, thus the use of buffer are minimized or even eliminated, reducing power consumption and minimizing routing paths.

Despite all benefits, the use of transistor networks flow are slowly than traditional standard cell approach. However, with newest technologies of distributed processing, this long time can be softened, getting possible the use of this kind of design flow in current designs, mainly for those that need a deep optimization in relationship with power.

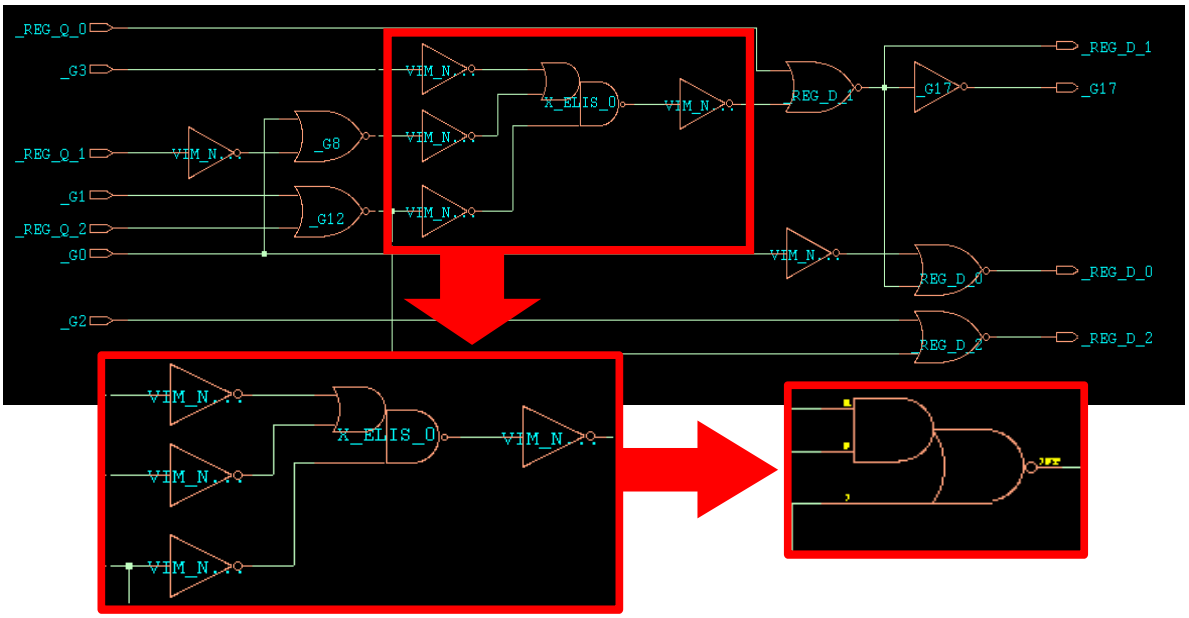

Figure 3: Schematic representation of the circuit S27a from Benchmark ISCAS89 exemplifying a deep optimization in the circuit.

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