Optimisation is a Keyword in IoT

Ricardo Reis
Optimisation is a keyword in IoT

Outline

Introduction
Optimisation at Different Abstract Levels
Optimisation of Computer Architectures (SoC)
Optimisation at Physical Design
Power Consumption Optimisation
Reliability
Conclusions
Internet of Things
Internet of Things

Includes

Small Devices - small number of components
Big Devices - big number of components
Reliable Devices (for critical applications)
Non Reliable Devices (TV set)

But all demands power optimization
Internet of Things

demands more and more Hardware & Software Codesign
Internet of Things

- 4 billion Connected People
- $4 trillion Revenue Opportunity
- 25+ million Apps
- 25+ billion Embedded and Intelligent Systems
- 50 trillion GBs of Data

Source: Mario Morales, IDC
Global Semiconductor Market

Sources: World Semiconductor Trade Statistics (WSTS) and SIA

Global Semiconductor Sales in May 2018 Increase 21% Year-to-Year
Internet of Things
Internet of Things

SERVICES SECTORS

Building
Energy
Consumer & Home
Healthcare & Life Sciences
Industrial
Transportation
Retail
Security & Public Safety
IT & Networks
The Internet of Things
An Explosion of Connected Possibility

1980: 1,000,000
1990: 0.5 Billion
2000: IoT Inception
2010: 8.7 Billion
2014: 14.4 Billion
2016: 22.9 Billion
2019: 34.6 Billion
2020: 50.1 Billion

Image Credit: The Connectivist
Internet of Health (IoH)

Glasses - advise eye correction

Toothbrush - find cavities, bad breath,…

Razor - identify acnes

Underwearables - early detection of cancer and other anomalies

Pacemaker - broadcast data to cardiologist
Internet of Health (IoH)

Combs - scan for fungus, hair loss, ...

Earphones - measurement of hearing, analysis of emotional level, ...

Watches - measurement of parameters like blood pressure, heart rate, ...

CHIP in Body

implanted chip in humans to monitor health parameters
Cyber Physical Systems

Systems composed of

electronic elements,
mechanical elements,
optical elements,
physical sensors,
chemical sensors,
organic elements,
and
many other type of components
1 sextillion in 2017

13 Sextillions Transistors Produced from 1947 to 2018

Source: SIA
A grain of rice has the price of more than a 125 thousand transistors.

Source: The Economist, September 6, 2010

A transistor is cheap

BUT

Energy is expensive

Power is related to Reliability
How much Power Plants we will need to cope with the IoT/IoE world?

It is Major Issue
Keyword in IoT

Optimisation
Optimisation must be done in all levels of abstraction from Software to Hardware Implementation
Do you how to do a green software?
Optimisation

Example:

Load: 10010011
Add: 10110011
Power consumption bigger than power dissipation capability
Hot Spot Reduction

To

Increase Reliability and Chip Life
Hardware Accelerators
APPLE8

2 Billions of transistors
TSMC 20 nm
89 mm²

FromDavidBrooks,Harvard,2014
The neural network hardware can perform up to 600 billion operations per second

6 CPUs
3 GPU
And lots of Hardware Accelerators
6.9 Billion transistors

TSMC 7 nm FinFet
9.89 x 8.42 mm = 83.27 mm²

NPU - Neural Processing Unit
8-core Neural Engine

6 CPUs
4 GPU
And lots of
Hardware Accelerators
Apple A12 Bionic - System on Chip

- 6 CPUs
- 4 GPU
- And lots of Hardware Accelerators
8.5 Billion transistors

TSMC 7 nm FinFet 2nd generation
10.67 mm x 9.23 mm = 98.48 mm²

18.27% die size increase
when compared to the previous A12

NPU- Neural Processing Unit with 8 cores
4 GPUs
4 CPU Thunder @ 1.8 GHz
2 CPU Lightning @ 2.65 GHz
Cache 8Mb

2666 MHz

And lots of
Hardware Accelerators
must be done in all levels of design abstraction

Power Estimation Tools for each level of abstraction
DARK SILICON
ENERGY HARVESTING
Medical Applications

ENERGY HARVESTING

Dedicated Chips

Ultra Low Power

Reliability
Transport Applications

Dedicated Chips

Reliability
Design Levels of Abstraction

Estimation Tools

Verification Tools

System

Modules

Logic Gates

Circuit

Devices

Trends

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In Modern Technologies

LESS TRANSISTORS MEANS LESS STATIC POWER
Example

\[ S = A + ((B + C) + D) \]

14 Transistors
Use of SCCG

\[
S = A + ((B + C) + D)
\]

\[
S = A + ((B + C).D)
\]

8 Transistors
Use of SCCG

\[ S = A + ((B + C) + D) \]

\[ S = A + ((B + C) \cdot D) \]

14 Transistors

8 Transistors
LESS CONNECTIONS ALSO MEANS MORE SPACE BETWEEN CONNECTIONS

Reliability Increases
Cell-internal EM – INV_X4 (45nm NANGATE)

J is 2.43X larger and the lifetime is 2.78X smaller (22nm technology)
Conclusions

more & more

IoT/ IoE world demands

Dedicated Chips
Low Power Chips
Conclusions

Optimization is a key point in NanoCMOS and in the IoT and IoE world, mainly power optimization.
Conclusions

more & more

Everything ends in a Chip
Conclusions

Countries that want to be an actor in the IoT/IoE world must have knowledge in transforming ideas into dedicated chips.
Something Else
Abstract:
Latin America has been far from high tech R&D centers, they are located mostly in Europe, Asia, and North America. However in 2006 Synopsys opened an R&D Center in Chile, after 14 years the center has more than 100 engineers developing EDA tools that are used by the most important semiconductor and electronic companies. Synopsys was the first EDA company that arrived to our Latin American region and today we can see that the 3 most important EDA companies are in the region, Synopsys and Mentor in Chile and Cadence in Brazil. During the talk we will analyze the factors that Synopsys analyzed in 2006 when they opened the center and the how the center has grown. We will also present what the center is doing and in which projects they are involved. We will end the presentation showing the key factor of success that we have learnt over the years.

Short CV:
Victor Grimblatt has an engineering diploma in microelectronics from Institut National Polytechnique de Grenoble (INPG – France) and an electronic engineering diploma from Universidad Tecnica Federico Santa Maria (Chile). He has expertise and knowledge in business and technology and understands very well the trends of the electronic industry; therefore, he is often consulted for new technological business development. He has published several papers in IoT, EDA and embedded systems development, and he has been invited to several events (Argentina, Brazil, Chile, Mexico, Peru and Uruguay) to talk about Circuit Design, EDA, IoT, and Embedded Systems. He is chair of the IEEE Chilean chapter of the CASS. He is also the President of the Chilean Electronic and Electrical Industry Association (AIE). He has been part of several conference TPCs (ISCAS, ICECS, LASCAS). Since 2018 he is Chair of LASCAS Steering Committee.
Design and Mitigation Methods for COTS FPGAs for Aerospace

Abstract:
FPGAs components are used in increasing quantities in both platform avionics and payload instruments. Several electrical, electronic and electromechanical rules must be guaranteed by FPGA components in Space especially to define the level of evaluation, screening and inspection necessary under radiation condition. The talk will cover aspects such as Performance, Area, Configurability/Programmability, Reliability, Radiation hardness (TID, SEUs, SETs, SEFIs, SEL and SEGR) and quality, packaging and mounting. The content of the presentation includes also data showing the different FPGA “eras” based on their architecture used in space ranging from the FPGA fabric to SoC FPGA.

Short CV:
Luca Sterpone received the MS and PhD degrees in computer engineering from Politecnico di Torino, Italy, in 2003 and 2007, respectively. He is currently an associate professor and deputy director with the Department of Computer Engineering, Politecnico di Torino. His current research interests include reconfigurable computing, computer-aided design algorithms, fault tolerance architectures and radiation effects on components and systems. He is author of more than 180 papers and he received several awards for his research activities. He is a member of the IEEE.
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