Exercício 10:

```
----------------------------------------------------------------------------
library ieee;
use ieee.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;

entity contador is
port(
   clk, up, down, cp, reset: in std_logic;
          input: in std_logic_vector(15 downto 0);
          output: out std_logic_vector(15 downto 0)
         );
end contador;

architecture behavior of contador is

signal buf00: std_logic_vector(15 downto 0);

begin

process (clk, reset)
        begin
                if(reset = '1') then
                        buf00 <= "0000000000000000";
                elsif (clk'event and clk = '1') then

                        if (up='1') then
                                buf00 <= buf00 + 1;
                        end if;

                        if (down='1') then
                                buf00 <= buf00 - 1;
                        end if;

                        if (cp = '1') then
                                buf00 <= input;
                        end if;

                end if;
end process;

output <= buf00;

end behavior;

----------------------------------------------------------------------------
```

Exercício 11:

```
----------------------------------------------------------------------------------
library ieee;
use ieee.std_logic_1164.all;

entity Reg8 is
port(
   clk, de, dd, cp, H: in std_logic;
          in0, in1, in2, in3, in4, in5, in6, in7: in std_logic;
          out0, out1, out2, out3, out4, out5, out6, out7: out std_logic
         );
end Reg8;

architecture behavior of Reg8 is

signal buf0, buf1, buf2, buf3, buf4, buf5, buf6, buf7: std_logic;

begin

process (clk)
        begin
                if (clk'event and clk = '1') then
                        if (cp='1') then
                                buf0 <= in0;
                                buf1 <= in1;
                                buf2 <= in2;
                                buf3 <= in3;
                                buf4 <= in4;
                                buf5 <= in5;
                                buf6 <= in6;
                                buf7 <= in7;
                        end if;

                        if (de='1') then
                                buf0 <= buf1;
                                buf1 <= buf2;
                                buf2 <= buf3;
                                buf3 <= buf4;
                                buf4 <= buf5;
                                buf5 <= buf6;
                                buf6 <= buf7;
                                buf7 <= '0';
                        end if;

                        if (dd='1') then
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```
                    buf0 <= '0';
                    buf1 <= buf0;
                    buf2 <= buf1;
                    buf3 <= buf2;
                    buf4 <= buf3;
                    buf5 <= buf4;
                    buf6 <= buf5;
                    buf7 <= buf6;
                end if;

                if (H = '1') then
                    buf0 <= buf0;
                    buf1 <= buf1;
                    buf2 <= buf2;
                    buf3 <= buf3;
                    buf4 <= buf4;
                    buf5 <= buf5;
                    buf6 <= buf6;
                    buf7 <= buf7;
                end if;

            end if;
end process;

out0 <= buf0;
out1 <= buf1;
out2 <= buf2;
out3 <= buf3;
out4 <= buf4;
out5 <= buf5;
out6 <= buf6;
out7 <= buf7;

end behavior;
--------------------------------------------------------------------------------
```