UNIVERSIDADE FEDERAL DO RIO GRANDE DO SUL
INSTITUTO DE INFORMÁTICA
PROGRAMA DE PÓS-GRADUAÇÃO EM COMPUTAÇÃO

Single Event Upset Mitigation Techniques for Programmable Devices

by

Fernanda Gusmão de Lima

Exame de Qualificação
EQ-02 PPGC-UFRGS

Prof. Ricardo Augusto da Luz Reis
orientador

Porto Alegre, 14 de dezembro de 2000

Table of Contents

List of Figures

List of Tables

Abbreviations and Glossary

ASIC	Application Specific Integrated Circuits
CMOS	Complementary Metal-Oxide-Semiconductor
COTS	Commercial of the Shelf
DUT	Device Under Test
EDAC	Error Detection and Correction
FPGA	Field Programmable Gate Array
IC	Integrated Circuits
LET	Linear Energy Transfer
LUT	Lookup Table
MPGA	Masked Programmable Gate Arrays
MPTB	Microelectronics and Phonics Test Bed
PLD	Programmable Logic Devices
SEE	Single Event Effects
SEL	Single Event Latchup
SEU	Single Event Upsets
SOI	Silicon on Insulator
TID	Total Ionization Dose
TMR	Triple Modular Redundancy
ULG	Universal Logic Gate
VHDL	VHSIC Hardware Description Language
VLSI	Very Large Scale Integration

Abstract

This report addresses the problem related with the use of standard CMOS digital circuit in space applications. Digital circuits especially those designed using sub-micron technologies operating in space environment are perturbed by charged particles. The charged particles can affect the circuit in different ways. This work details one of these effects called Single Event Upset (SEUs).

During a single event upset, a single charged particle strikes the silicon, generating a transient pulse of current that can produce a bit flip in a memory cell. This transient current pulse can provoke a functional fault in the circuit. This work is a study of SEU mitigation techniques for CMOS digital circuits. There are three main approaches to avoid radiation upsets in digital circuits. The first one is hardening by technology where a specific technology process is used to turn the circuit SEU immune. The second one is hardening by design where the structure of the memory cell is modified to turn it hardened. This report addresses some developed solutions to turn CMOS memory cells SEU immune showing some advantages and drawbacks. The third solution is hardening by system where software solutions and hardware redundancy is used to SEU mitigation. Each one has advantages and drawbacks that are discussed in this report.

Programmable Logic Devices are widely used to implement digital circuits by offering the advantage of fast turnaround time, comparing to custom ASICs which present high recurring engineering cost and high risk, especially in limited production volume. They include Masked Programmable Gate Arrays (MPGAs) and Field Programmable Gate Arrays (FPGAs). However, the high number of latches presented in these circuits turns the programmable devices strongly sensitive to radiation. Consequently they must be protected to avoid errors when used in space applications. This report presents some techniques used nowadays to avoid SEU in MPGAs and commercial FPGAs.

PART I: Microelectronics Circuits under Radiation

1 Introduction

The increase on the use of the space systems, whether they are military, research, or commercial missions, in this new millennium is due to the constant expansion necessity of information, communication and science research.

In the 1970s the view was widely held that designing radiation-hardened spacecraft and systems would become a “non-problem” with the development of radiation-hardened electronic components. Unfortunately that is not the reality of today. In fact, reducing radiation effects on spacecraft systems to manageable levels is more complex than ever. There are currently no completely radiation hardened devices in existence. The need for a system with high levels of performance has exceeded the capabilities of available radiation hardened components and technology. At the same time, the demand for electronics goods in commercial markets has greatly decreased the manufacturer’s interest in developing radiation hardened components, driving up the cost of radiation hardened parts and making them increasingly unavailable. [BAR97]

The radiation hardened market share is still too small. The decreased support for radiation hardened component design and technology in the military sector in the last few years has compounded the problem. Increasingly, system performance requirements must be met by using commercial technologies that have complex responses to the radiation environment. [BAR97]

Microelectronic industry has advanced in the last few years designing more and more complex and high density integrated circuits (ICs). The reason for the increase in density and performance is largely due to the decreasing of transistor feature sizes (minimum gate length of a CMOS transistor). Transistor gate length in commercial ICs have shrunk from 1.0 micron (several years ago) to 0.18 microns (nowadays) and continue to shrink to a projected 0.05 microns (by the year 2012). [SIA94]

Space applications, such as satellites, probes, shuttles and others widely use microelectronic devices. Advanced integrated circuits (high-density, high-performance and low power) are becoming extensively used in space environment in order to meet spacecraft requirements such as size, weight, power and cost. However, these circuit advances, by their very nature, increase the vulnerability of the devices due to the size of the gate transistors and to the small capacitance used to store signals.

The design of digital circuits for space application needs first to consider the space radiation environment and the target orbits. It is essential to study the radiation effects in digital circuits and the ways to qualify these digital circuits for space applications.

In space, integrated circuits are subjected to hostile environments composed of a variety of particles including photons, charged particles, neutrons and others. The charged particles can hit the ICs resulting in non-destructive or destructive effects according to the charge intensity and to the hit location.

Radiation effect problems in space applications can be tackled by:

- using radiation hardened devices,
- qualifying commercial circuits by radiation ground testing.

Using radiation hardened devices will often solve the radiation effects problem. However, these devices are much more expensive than a non-hardened device. Not every device is available in a hardened version and hardened devices are usually fabricated using non state-of-art technologies.

Current policies of Space Agencies (NASA, ESA, etc) favor the insertion of Commercial Of-The-Shelf (COTS) technologies in the design of their systems. Thus, an alternative solution is to carefully select candidate devices by choosing only those which are robust enough to cope with the environment requirements. Qualifying these devices involves radiation ground testing to determine if they will survive in the radiation environment of the target orbit. The results of the radiation ground testing are used to extrapolate the device's survivability in the particular orbit of interest. Many times this extrapolation underestimates survivability and devices that could survive are not used. A more dangerous possibility occurs when survivability is overestimated increasing the possibility of a device failure in orbit.

The main problem addressed in this work is the design of robust integrated circuits for space applications based on standard commercial process technologies.

The first part of this report focuses the problem of using digital circuits in space application. This part is divided into 6 sections. Section 2 presents the space radiation environment. Section 3 shows the radiation effects on digital circuits. Section 4 exemplifies some methodologies to test digital circuits for space applications. Section 5 addresses some methods to mitigate single event upsets. According to these techniques, some hardened memory cells applicable for standard CMOS digital circuits are presented in section 6. A comparison of the efficiency between these memory cells is then contributed.

The second part of this report presents programmable circuits devices used in space applications. Programmable circuits can be Masked Programmable Gate Arrays (MPGAs) or Field Programmable Gate Arrays (FPGAs). These approaches are addressed in section 7. Section 8 discusses some mitigation solutions for MPGA devices. Section 8 presents some mitigation solutions for FPGA devices. These solutions can be obtained at circuit level, at design level or at system level. All these solutions must consider the type of FPGA. Section 10 presents the main conclusions.

2 Space Environment

The space environment consists of various particles that may interact with digital microelectronic devices causing undesirable effects. Particles of concern are electrons, protons, photons, alpha particles and heavier ions [STA88].

The space particles can be classified into two primary categories:

- photons
- charged particles

The photon particles have zero rest mass and are electrical neutral. They interact with target atoms producing energetic free electrons. The charged particles interact with the silicon atoms causing excitation and ionization of atomic electrons.

The main sources of charged particles, illustrated in figure 2.1 [BAR97], that contribute to radiation effects are:

- protons and electrons trapped in the Van Allen belts,
- heavy ions trapped in the magnetosphere,
- galactic cosmic ray protons and heavy ions,
- heavy ions and protons from solar flares.

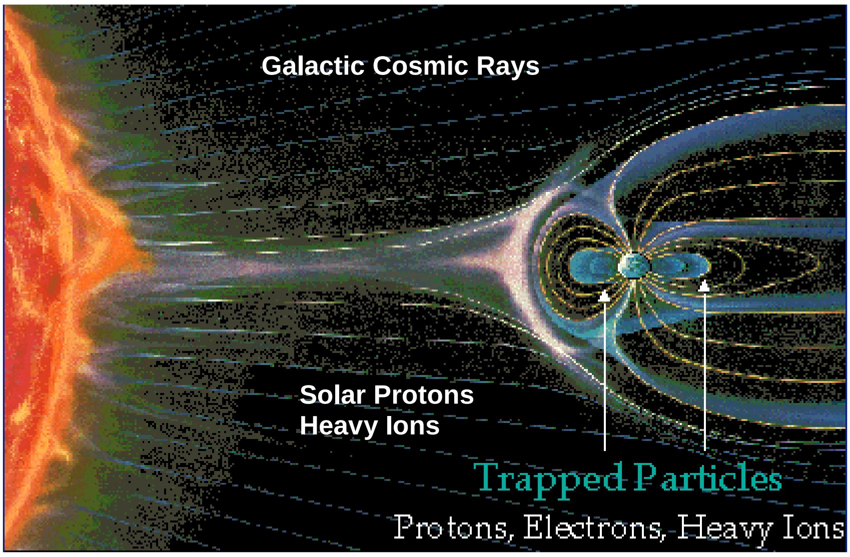


Figure 2.1 – Charged particles in the space environment

The levels of all of these sources are affected by the activity of the sun. The solar cycle is divided into two activity phases: the solar minimum and the solar maximum. The cycle lasts about eleven years, with approximately four years of solar minimum and seven years of solar maximum. Table 2.1 shows the abundance of some particles in the solar wind.

Table 2.1 – Solar wind particle composition

Particle	Abundance
Proton	95% of the Positively Charged Particles
He ++	~4% of the Positively Charged Particles
Other Heavy Ions	< 1% of the Positively Charged Particles
Electrons	Number Needed to Make Solar Wind Neutral

There are also extremely large variations in the levels of radiation effects inducing flux that a given spacecraft encounters, depending on its trajectory through the radiation sources. Missions flying at Low Earth Orbits (LEOs), Highly Elliptical Orbits (HEOs), Geostationary Orbits (GEOs), and planetary and interplanetary missions have vastly different environmental concerns. [BAR97]

- *Low Earth Orbits (LEOs)*: Satellites in LEOs pass through the particles trapped in the Van Allen belts several times each day. The level of fluxes seen during these passes varies greatly with orbit inclination and altitude. The location of the peak fluxes depends on the energy of the particle. For protons with E > 10 MeV, the peak is at about 3000 km. For normal geomagnetic and solar activity conditions, the flux level drops rapidly at altitudes over 3000 km. However, high-energy protons have been detected in the regions above 3000 km after large geomagnetic storms and solar flare events.
- *Highly Elliptical Orbits (HEOs):* Highly elliptical orbits are similar to LEO orbits, they pass through the Van Allen belts each day. However, because of their high altitude, they also have long exposures to the cosmic ray and solar flare environments regardless of their inclination. The levels of trapped proton fluxes that HEOs encounter depends on the perigee position of the orbit including altitude, latitude, and longitude. If this position drifts during the course of the mission, the degree of drift must be taken into account when predicting proton flux levels. HEOs also accumulate high total ionization dose levels due to both the trapped proton exposure and the electrons in the outer belts where the spacecraft spends a significant amount of time during each apogee pass.
- *Geostationary Orbits (GEOs):* At geostationary altitudes, the only trapped protons that are present are below energy levels necessary to initiate the nuclear events in materials surrounding the sensitive region of the device that cause SEEs. However, GEOs are almost fully exposed to the galactic cosmic ray and solar flare particles. Protons below about 40-50 MeV are normally geomagnetically attenuated, but this attenuation breaks down during solar flare events and geomagnetic storms. Field lines that are at

about 7 earth radii during normal conditions can be compressed down to about 4 earth radii during these events. As a result, particles that were previously deflected have access too much lower latitudes and altitudes. Also, GEO satellites are continuously exposed to trapped electrons, hence, the total dose ionization accumulated in GEO orbits can be severe for locations on the satellite with little shielding.

- *Planetary and Interplanetary*: The evaluation of the radiation environment for these missions can be extremely complex depending on the number of times the trajectory passes through the earth's radiation belts, how close the spacecraft passes to the sun, and how well known the radiation environment of the planet is. Each of these factors must be taken into account very carefully in the exact definition of a mission trajectory.

The trapped ions located in the Van Allen belts are shown in figure 2.2 [BAR97]. The trapped eletrons in the Van Allen belts are located into inner zones and outer zones populations. The inner zone electrons are less severe compared to the outer zone electrons.

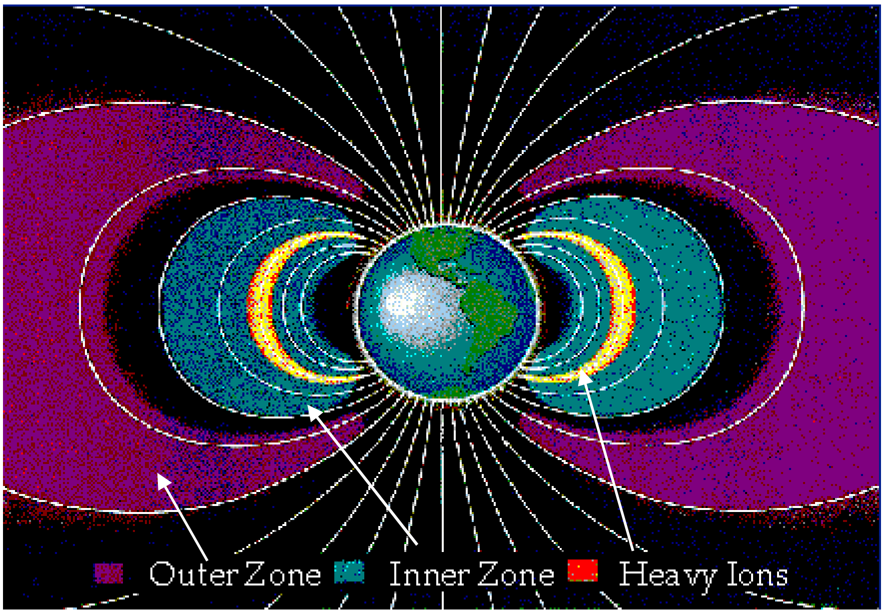


Figure 2.2 – Trapped particles in Van Allen belts

Figure 2.3 shows the proton and electron intensity in the Van Allen belts according to the NASA AP-8 and AE-8 models. (The “A” is for Aerospace Corporation.). The AP-8 and AE-8 models include data from 43 satellites, 55 sets of data from principal investigator instruments, and 1,630 channel-months of data. These models are empirical data sets for static conditions. The energy range of the protons included in the AP-8 is 0.04 to 500 MeV. The energy range in the AE-8 electron model is 0.04 to 7.0 MeV.

Figure 2.4 and figure 2.5 [BAR97] show the trapped proton and electron energy respectively according to the altitude.

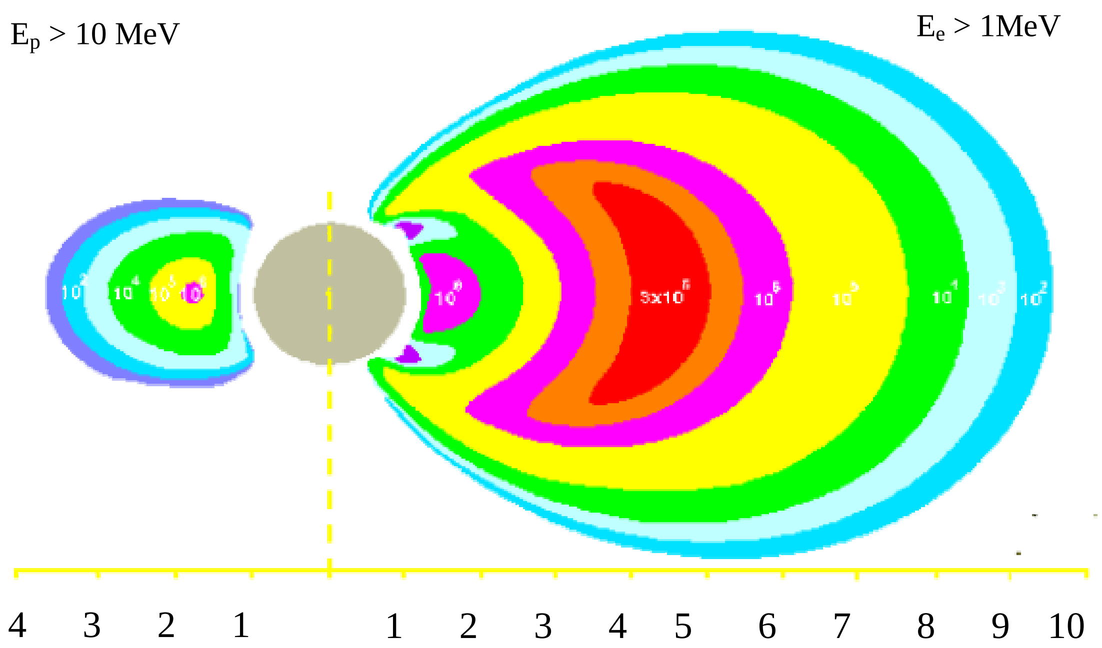


Figure 2.3 – Proton and electron intensities in Van Allen belts

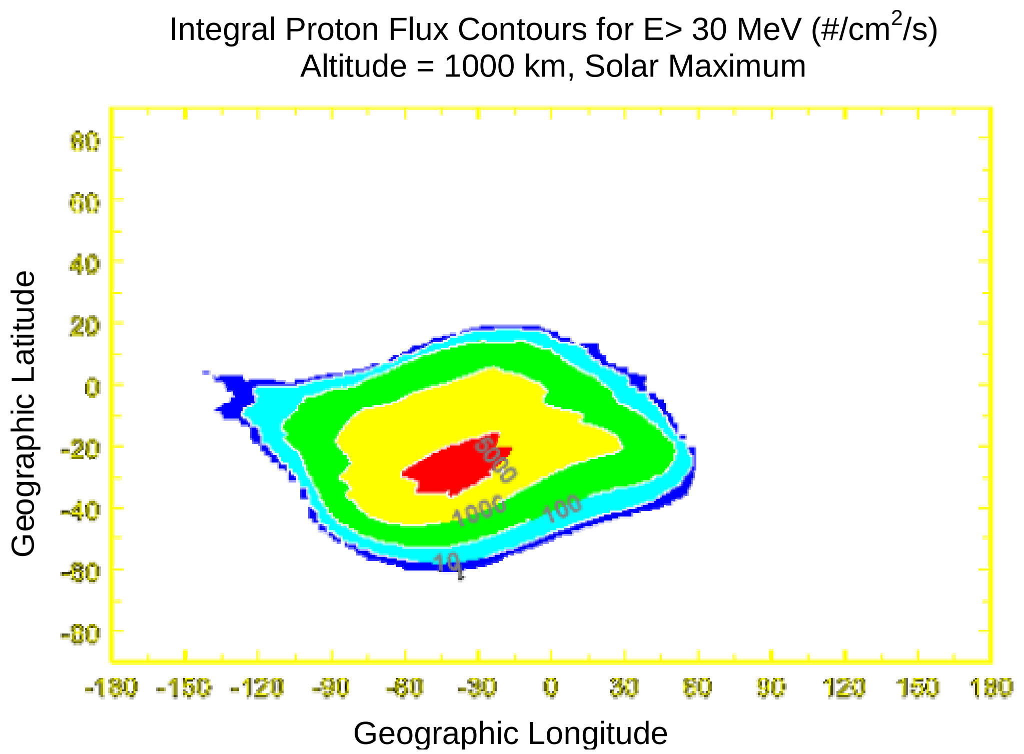


Figure 2.4 – Trapped proton energy - 1000Km [BAR97]

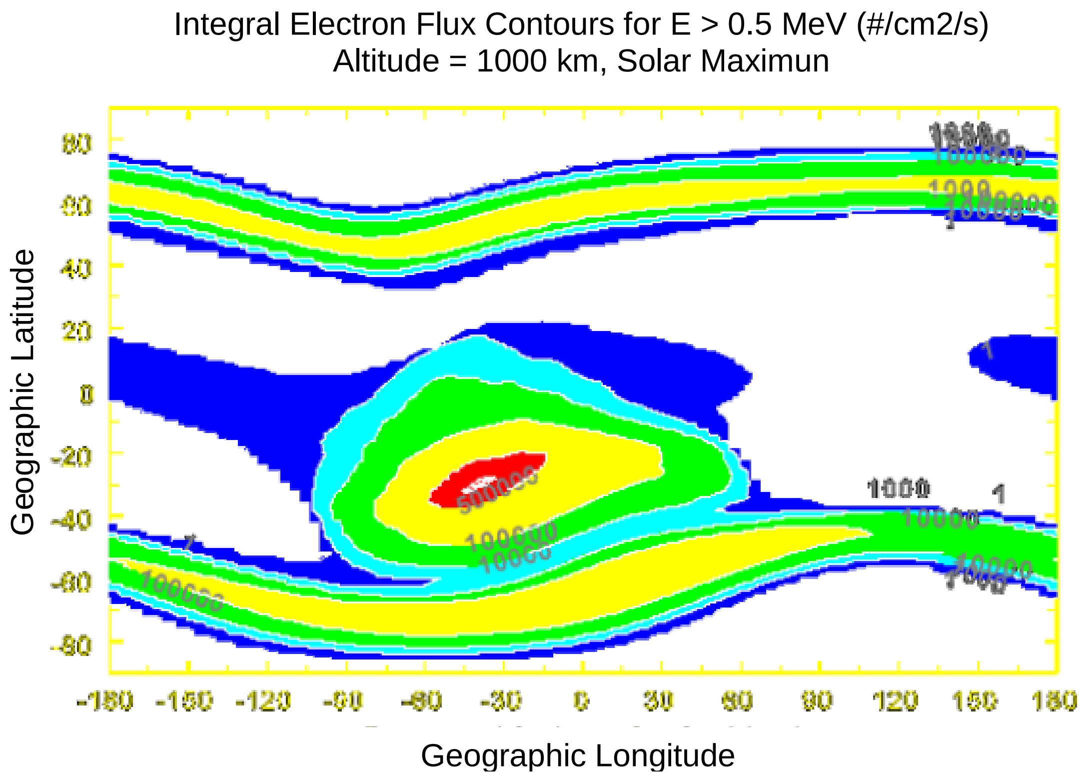
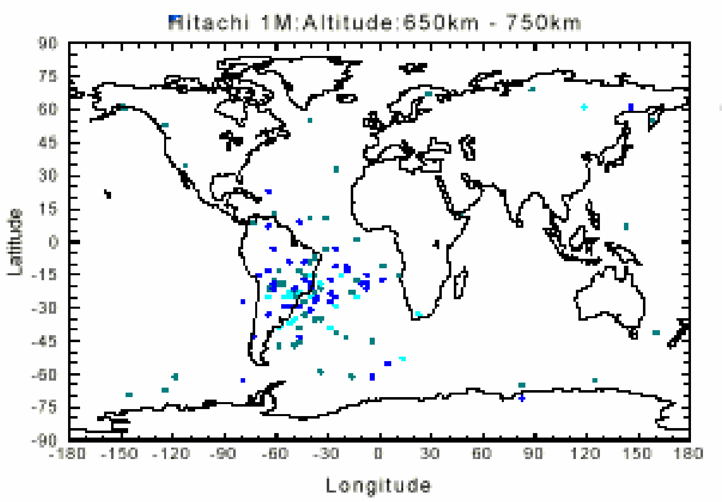


Figure 2.5 – Trapped electron energy - 1000Km

In the Low Earth Orbits (LEO), the most intense and penetrating radiation is encountered in the form of protons in the South America Anomaly (SAA). The SAA is responsonsible for most of the trapped radiation received in low earth orbits. There, the Van Allen belts reach lower atitudes, extending down into the athmosphere. Figure 2.6 [BAR97] shows the trapped particles in the world according to the altitude of the orbits.



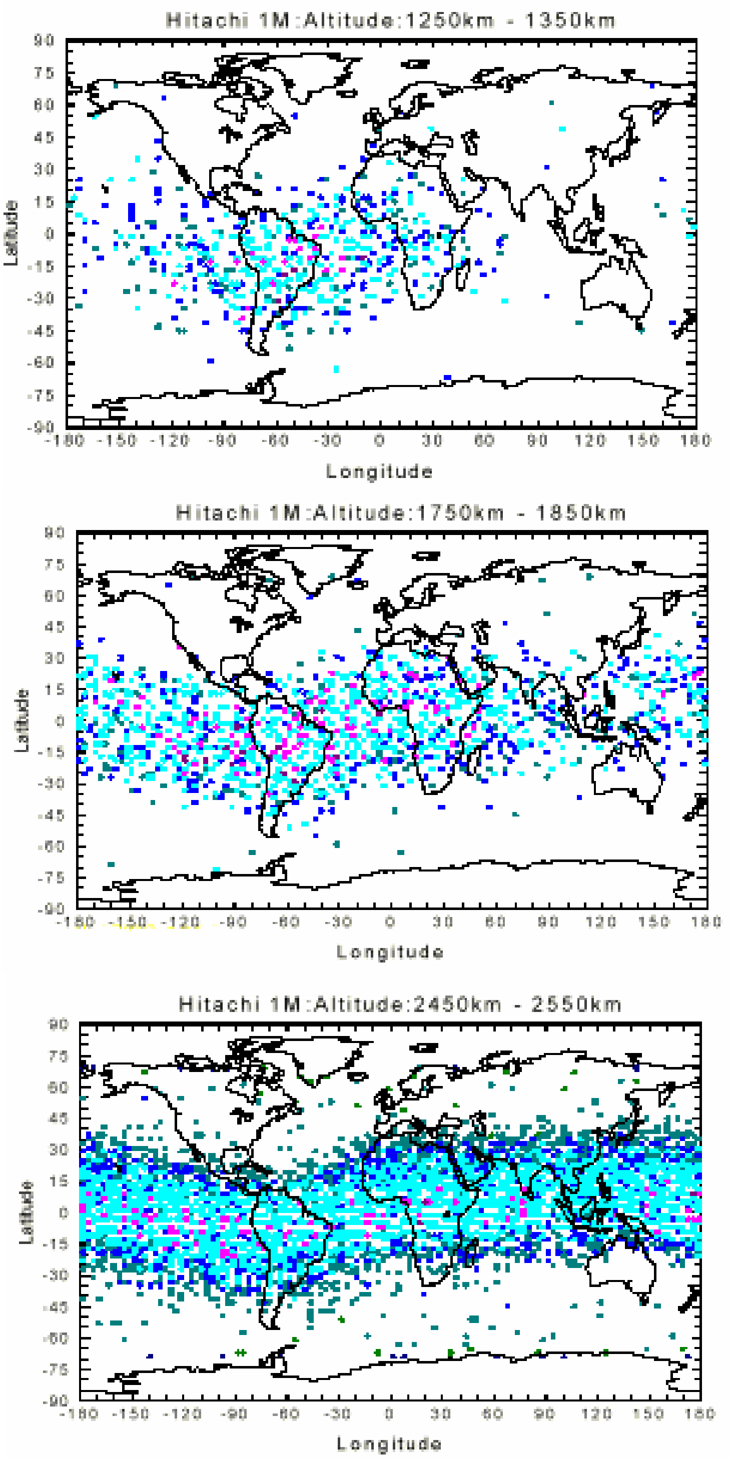


Figure 2.6 – SRAM upsets rates in South America Anomaly (SAA)

The trapped particles gyrate around and bounce along the magnetic field lines, and are reflected back and forth between pairs of conjugate mirror points (i.e., regions of maximum magnetic field strength along their trajectories) in opposite hemispheres. At the same time, because of their charge, electrons drift eastward around the earth, while protons and heavy ions drift westward. Figure 2.7 [BAR97] shows the motions of trapped particles in an orbit.

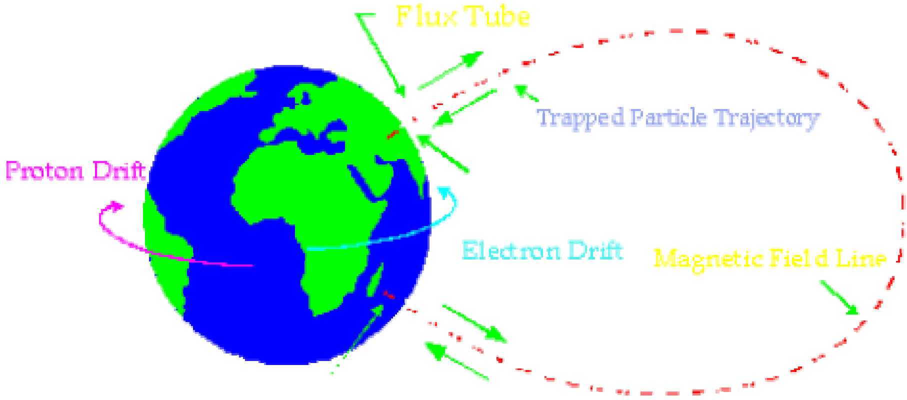


Figure 2.7 – Motions of trapped particles

Spacecraft have to be able to operate in the Earth's radiation belts to carry out their mission. The microelectronic and photonic devices can be perturbed or even destroyed by the natural space radiation environment. The charged particles can affect the digital devices in different ways according to their intensity and to the interaction location. The radiation effects are addressed in the next section.

In the near future, due to the constantly progress in CMOS technologies which lead to decreasing transistors features (gate dimensions and voltage supplies), the neutron particles presented in the atmosphere will be able to affect digital logic circuits operating on ground applications [NOR96].

When cosmic ray particles enter the top of the atmosphere, they are attenuated by interaction with nitrogen and oxygen atoms. The result is a “shower” of secondary particles and interactions created through the attenuation process. Products of the cosmic ray shower are protons, electrons, neutrons and heavy ions. Figure 2.8 shows the Neutron Environment.

The knowledge of neutron levels comes from balloon, aircraft, and ground based measurements [BAR97]. Ground-based studied have shown that the variation in the neutron flux level is measurable when the altitude ranges from sea-level to mountainous regions.

Figure 2.9 [BAR97] shows the measured neutron flux normalized to the peak versus altitude for two energy ranges, E = 1 - 10 MeV and 10 - 100 MeV.

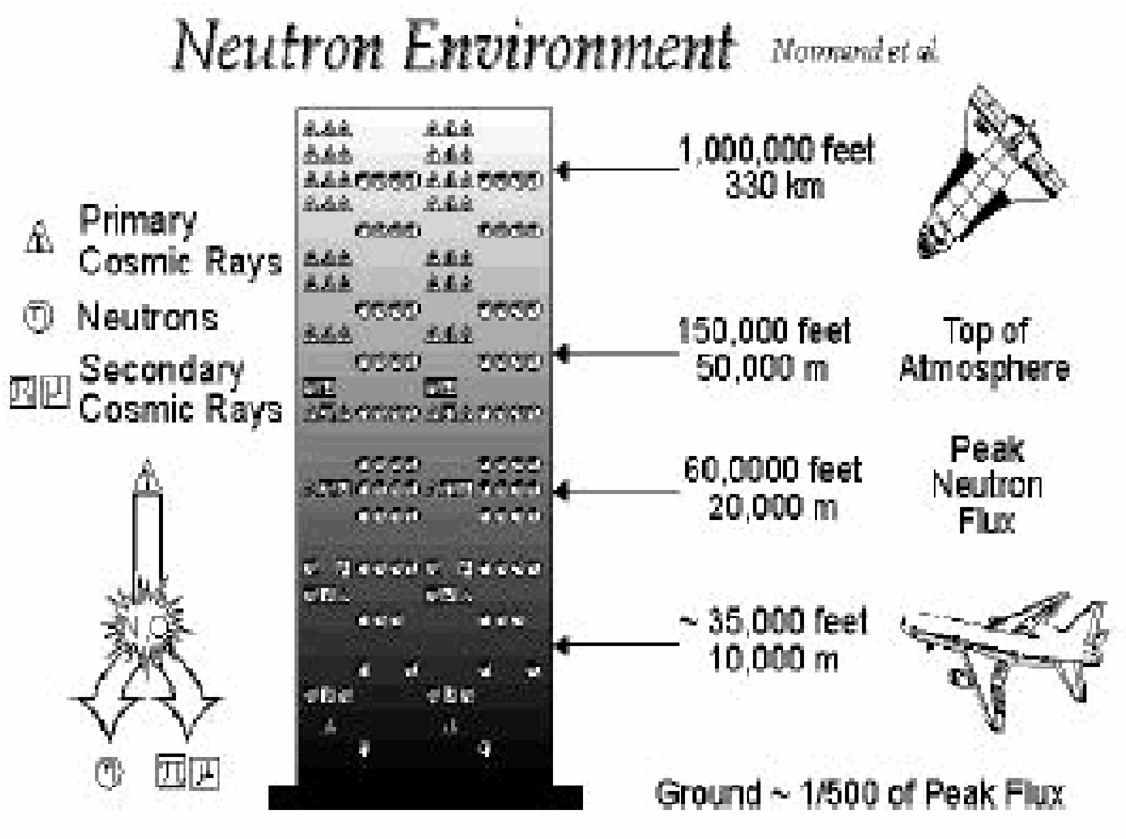


Figure 2.8 – Neutron environment

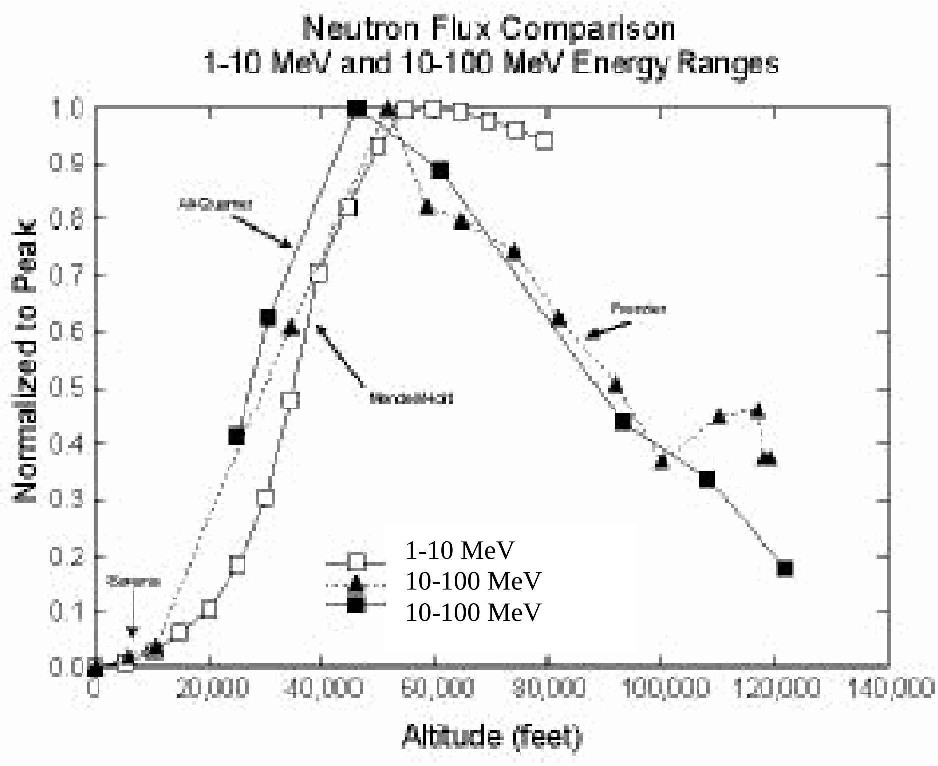


Figure 2.9 – Measurements of atmospheric neutrons show the variation as a function of altitude

Table 2.2 summarizes the radiation environment that must be accounted in radiation effects analyses and in the models that provide predictions of the radiation environment.

Table 2.2 – Summary of radiation sources

Particle Origin	**Particle Type**	**Effects of Solar Cycle**	**Variations**	**Types of Orbits Affected**
Trapped	Protons	Solar Min - Higher; Solar Max - Lower	Geomagnetic Field, Solar Flares, Geomagnetic Storms	LEO, HEO, Transfer Orbits
	Electrons	Solar Min - Lower; Solar Max - Higher	Geomagnetic Field, Solar Flares, Geomagnetic Storms	LEO, GEO, HEO, Transfer Orbits
Transient	Galactic Cosmic Ray Ions	Solar Min - Higher; Solar Max - Lower	Ionization Level, Orbit Attenuation	LEO, GEO, HEO
	Interplanetary Solar Flare Protons	During Solar Max Only	Distance from Sun; Outside 1 AU, Orbit Attenuation; Location of Flare on Sun Interplanetary	LEO (I>45°), GEO, HEO, Solar Flare
	Heavy Ions	During Solar Max Only	Distance from Sun; Outside 1 AU, Orbit Attenuation; Location of Flare on Sun	LEO, GEO, HEO, Interplanetary
Secondary	Neutron-Atmospheric	Solar Min - Higher; Solar Max - Lower	Barometric Pressure Solar events	Aircraft Altitudes, Space Shuttle Ground Level
	Neutron – Aircraft Shielding	Solar Min - Higher; Solar Max - Lower	See trapped protons	See trapped protons

3 Radiation Effects on Digital Circuits

The digital circuits located in the space environment are affected by the charged particles generated by the solar flares. As higher is the performance of a circuit more sensitive to radiation environment it is. High-density devices require smaller feature size, this means less capacitance and hence information is stored with less charge. Lower voltage or lower power devices means that less charge or current is required to store information. Each of these effects makes the device more vulnerable to radiation and means that particles with little charge, which were once negligible, are now much more likely to produce upset or damage.

Two classes of radiation effects must be considered when developing Very Large-Scale Integrated (VLSI) circuits devoted to be included in space projects [LAB99]:

- Total Ionizing Dose (T.I.D.),
- Single Event Effects (S.E.E.).

T.I.D. is due to the long-term degradation of electronics due to the cumulated charge deposited in a material. Electronic devices suffer long-term radiation effects, mostly due to electrons and protons. The main sources of these particles are Solar Energetic Particle Events - which usually occur in association with solar flares - and the South Atlantic Anomaly (SAA) - where the Earth's magnetosphere dips closest to the earth, causing more trapped radiation. In that time, devices can suffer threshold shifts, increased device leakage and power consumption, timing changes, decreased functionality, etc. Device shielding can help, but several factors must be considered. Shield geometry, analysis technique, shield material and device composition are all relevant in predicting shield effectiveness. Electrons can be effectively attenuated by aluminum shielding even at high energies. However, while aluminum shielding is effective for low-energy protons, it is ineffective for the high-energy protons (>30 MeV).

S.E.E. is a transient effect induced by the trespassing of a single charged particle through the silicon. A single charged particle strikes the material, ionizes it and provokes a current pulse that can be damage or not. Significant sources of SEE exposure in the space environment include trapped protons, solar protons, neutrons and heavy ions from galactic cosmic rays [BRY98].

Heavy ions trapped in the magnetosphere do not make a significant contribution to the TID but they have sufficient energies to penetrate the satellite and to generate the ionization necessary to cause SEEs.

Table 3.1 summarizes the effects of the particles in the radiation environment on spacecraft systems.

Table 3.1 – Radiation effects summary

Particle Origin	Particle	Effect
Trapped	Protons	Total Dose SEEs Displacement Damage Solar Cell Degradation
	Electrons	Total Dose Solar Cell Degradation
	Heavy Ions	Possible SEEs Dose Exposure for Humans
Transient	Solar Protons	Total Dose SEEs Displacement Damage Solar Cell Degradation
	Solar Heavy Ions	SEEs
	Galactic Cosmic Rays	SEEs Dose Exposure for Humans
	Plasma Electrons	Deep Dielectric Charging
Secondary	Neutrons-Atmospheric	SEUs in Avionics
	Neutrons-Spacecraft Shielding	Displacement Damage

Single Event Effects are divided into three main categories according to the consequence of the spurious current pulse:

- *Soft SEEs*: a radiation induced transient in a linear device, or a radiation induced bit upset in a digital device. Soft SEEs are not permanent; they are cancelled by resetting the system or by rewriting data in a memory.
- *Hard SEEs*: a SEE that causes a permanent change to the operation of a device. Example: stuck bit in a memory.
- *Destructive SEEs*: a SEE which causes the destruction of a device. Example: Single Event Latch- up (SEL), Single Event Gate rupture (SEGR), Single Event Burnout (SEB). SEB is a highly localized destructive burnout of the drain-source in power MOSFETs and SEGR is the destructive burnout of a gain insulator in a power MOSFET.

Soft errors called Single Event Upsets (SEU) occur when a charged particle hits the material provoking a transient pulse. This transient pulse can change the state of a memory cell. The consequences of SEUs are entirely device specific, and depend on the impact of the corrupted information in the system. In a combinational logic or analog-to-digital converter, a transient pulse in the device caused by a charged particle hit can be a potential SEU according to the performance of the circuit. In other hand, a transient pulse in a memory cell or latch will be a SEU because the transient current pulse will change the memory cell value.

The most common hard error is the Single Event Latchup (SEL) that is due to shorts between ground and power, and it causes permanent functional damages. Single Event Latchup (SEL) is a potential destructive condition involving parasitic circuit elements. During a SEL, the device current exceeds the maximum specified for the device. Unless power is removed, the device will eventually be destroyed by thermal effect. A micro latchup is a type of SEL when the device current is elevated, but below the device's specified maximum. In this case power reset is also required to recover normal device operation. Latchup occurs when a spurious current spike, such as that produced by a heavy cosmic ray, activates one of a pair of these parasitic transistors, which combine into a circuit with large positive feedback. The result is that the circuit turns fully on and causes a short across the device until the latter burns up or the power to it is cycled.

Table 3.2 shows a resume of different Single Event Effects classified by device and by sensitive areas [DEN00].

Table 3.2 – SEE categories by device and by sensitive areas

Device Type	Sensitive Area	SEU Types
Memories	Memory cells	Bit flips
	Control logic	Bit flips if sequential, transient if combinational
Combinational Logic	Combinational logic	Transient
Sequential Logic	Sequential logic	Bit flips
FPGAs	Combinational logic	Transient if combinational CLBs, bit flips if CLBs based on Lookup Tables (LUTs).
	Sequential logic	Bit flips
Microprocessors	Registers, caches, sequential, control logic	Bit flips
	Combinatorial logic	Transients
ADCs, DACs	Analog Portion	Transients
	Digital Portion	Bit flips or transient depending of the design
Linear ICs	Analog area	Transient
Photodiodes	Photodiode	Transient

This work focuses the effects of Single Event Upset in memories, sequential circuits in general such as microprocessors and programmable circuits such as FPGAs. Next section shows in more details these effects.

3.1 Single Event Upset (SEU)

Single Event Upsets are produced by single charged particles hits over integrated circuits. The SEU targets are drains of OFF transistor. When a single charged particle strike an integrated circuit element, it loses its energy via the production of electron hole pairs resulting in a dense ionized track in the local region. This ionization causes a transient current pulse [BES93]. Figure 3.1 illustrates this event.

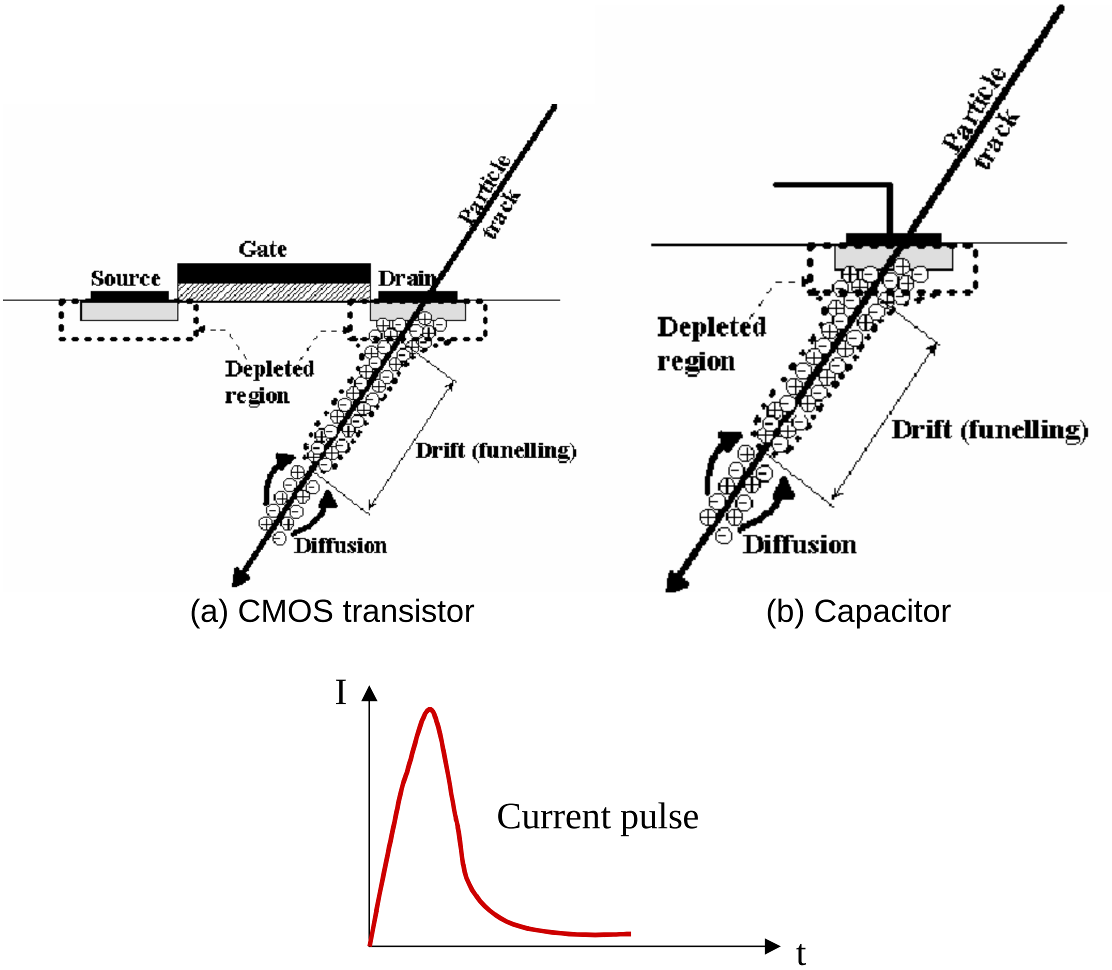


Figure 3.1 – Charge particle striking a silicon surface and generating a current pulse

The most common circuit sensitive to SEU is the memory element, figure 3.2. The memory cell is designed so that it has two stable states, one that represents a stored '0' and one that represents a stored '1.' In each state, two transistors are turned on and two are turned off (SEU target drains). A bit-flip in the memory element occurs when an energetic particle causes the state of the transistors in the circuit to reverse. This phenomenon occurs in many microelectronic circuits including memory chips and microprocessors. In a spaceborne computer, for example, a bit-flip could randomly change critical data, randomly change the program, or confuse the processor to the point that it crashes.

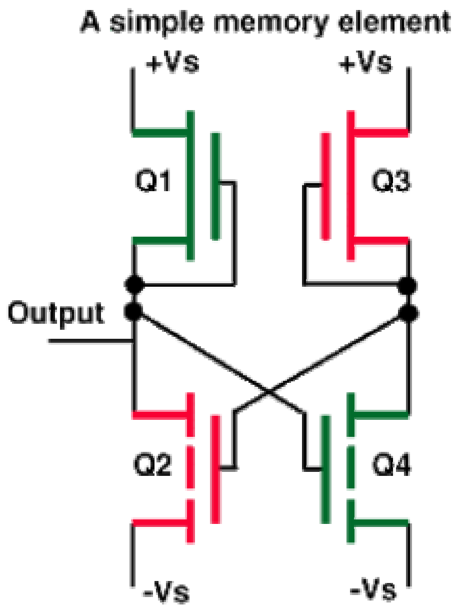


Figure 3.2 – SEU effects in a simple memory element

Charged particles can also induce transient current pulses in combinatorial logic, in global clock lines, and in global control lines. These single event transients (SETs) have only minor effects in present 0.8 to 0.7 micron technologies since the speed of these circuits is insufficient to propagate a 100 to 200 ps SET over any appreciable distance through the circuit. Figure 3.3 shows a typical sequential circuit topology.

An upset in the combinational logic can generate an error that is going to be stored in the flip-flop U2 if the speed of the circuit is high enough to propagate the error before the clock change the state of the flip-flop. If the speed is not high enough, the upset in the combinational logic will disappear before the clock change the state of the flip-flop U2, for example.

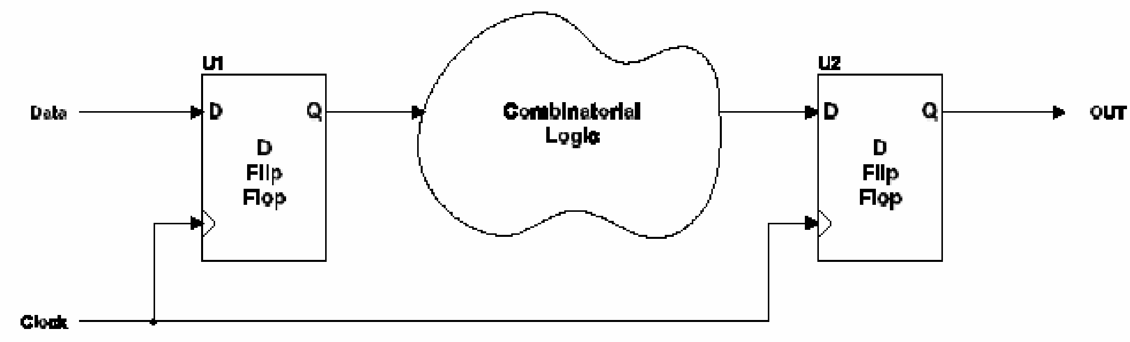


Figure 3.3 – Typical sequential circuit topology

However, as smaller feature size and thus faster technologies are becoming strongly used in spacecraft systems where transient pulses generated by charged particle hits can be indistinguishable from normal circuit signals, an upset in the combinational logic can be propagated fast to flip-flops input provoking errors in the circuit.

Another problem is the neutron particles presented in the atmosphere. The influence of the neutron particles in state-of-the-art technology circuits increases due to the small size of the gate transistors and to the low voltages as it was mentioned in last section. When a neutron hits a digital circuit with these characteristics, it also provokes a pulse of current that can be interpreted like a signal in the circuit. The perturbation results of the interaction of neutron atoms in the atmosphere and the Bo atoms existed in CMOS technologies. This problem may be concern digital logic device developments to avoid upsets in the functionality in both combinational and sequential logic in the atmosphere. Previous papers [BAR97] pointed out the hazard of single event upsets at avionics altitudes. They showed that, below altitudes of about 18 km, secondary neutrons from cosmic ray heavy ion fragmentation are the most important contributors to SEUs.

3.1.1 SEU measures

When a charged particle passes across any material it loses energy through interactions with the material. The energy lost is primarily due to the interactions of the ion with the bound electrons in the material, causing an ionization of the material and a dense track of electron-hole pairs. The rate at which the ion looses energy is called stopping power (dE/dx). The incremental energy dE is usually measured in units of MeV while the material thickness is usually measured as a mass thickness in units of mg/cm^2. [LAB99], [BRY98]

The amount of energy lost by the particle per unit path length is called *linear energy transfer* (LET) and varies directly as the square of the atomic number of the particle and inversely as its energy. Thus, the amount of energy deposited (and therefore, charge created) in a vulnerable region of a circuit component is proportional to LET versus path length in the region (mg/cm^2).

By counting the number of Single Event Effects and knowing how many particles passed through the part, we can calculate the probability of a particular particle causing a Single Event Effect. This resultant number, which is the number of upsets divided by the number of particles per cm^2 causing the upsets, is called the *cross-section* of the part and is measured in units of cm^2 / device.

Consequently, the S.E.E. sensitivity of a device is by a function of the Cross Section (σ) in terms of L.E.T. *(Linear Energy Transfer*): σ (L.E.T.).

Resuming, LET *(*Linear Energy Transfer) is a measure of the energy deposited per unit length when an energetic particle travels through a material. The common unit is MeV*cm^2/mg of material (Si for MOS devices). The *LET threshold* (LETth) is the minimum LET to cause an effect. The Cross-Section σ(L.E.T.) is defined by the number of errors and the particle fluency (# Errors / particle fluency). Error Rate is defined as the number of errors per device per day. The error rate can be estimated from LETth, σ sat and parameters of the final orbit. Figure 3.4 shows the typed LET curve.

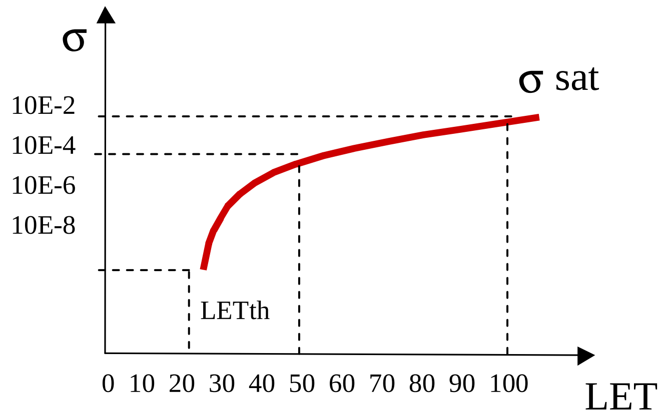


Figure 3.4 – A typed LET curve

Analyzing this curve, we can say that no error occurs in the presence of particles with LET (linear energy transfer) lower than 25 MeV. For particles with 25 MeV, it is necessary more than 100.000.000 particles per second travelling through the circuit sensitive area to occur one upset. For particles with 50 MeV, it is necessary 10.000 particles per second to occur one upset. And it is necessary a fluency of 100 particles per second with a LET of 100 MeV to occur one upset.

To analyze the SEU immunity of a device in the space environment, different SEU rates must be taken to account based on LETth as it is showed in table 3.3.

Table 3.3 – SEU rates device threshold

Device Threshold	***Environment to be Assessed***
LETth < 10 MeV*cm2/mg	Cosmic Ray, Trapped Protons, Solar Flare
LETth = 10-100 MeV*cm2/mg	Cosmic Ray
LETth > 100 MeV*cm2/mg	No analysis required

The SEU system-level impact depends on the type and location of the effect, as well as on the design. Since SEE presents a functional impact to a device, functional analysis enables the evaluation of effects. The design is viewed in terms of function, not by box or physical subsystem. Functions are categorized into "criticality classes", or categories of differing severity of SEE occurrence.

For example, in a design, there might be three critical groups for SEU:

- error-functional,
- error-vulnerable,
- error-critical.

Functions in the *error-functional* groups are unaffected by SEUs when protected by error-correction scheme or redundancy. Functions in *the error-vulnerable* group might be those to which the risk of a low probability is assumable. Functions in the *error-critical* group are functions where SEU is unacceptable and must be protected by SEE mitigation techniques.

Both the functional impact of a SEU at the system level and the probability of its occurrence provide the foundation for setting a design requirement. Unlike TID tolerances, SEE rates are probabilistic, given as a predicted span of time within which a SEE will randomly occur. Requirements are specific for each functional group specifying the maximum probability of SEU permitted in each category. Optimizing design for SEU tolerance is a trade between risk, cost, performance, and design complexity.

4 Radiation Test of Integrated Circuits

Testing integrated circuits in a severe radiation environment in advance to their use in operational systems is very important and it will help to reduce the probability of failures in future space applications.

The sensitivity evaluation of a circuit with respect to radiation can be done by:

- the analysis of flight data issued from spacecraft operating in the actual environment: space projects,
- ground testing,
- fault injection.

Before analyzing all the different ways to evaluate a device for space application, it is necessary to study the test methodology that can be applied for each evaluation.

4.1 Test Methodology

The test methodology depends on the Device Under Test (DUT) type. For example, the methodology used for memories consists mainly in to write a data pattern, to wait a loop read out and to compare to expected values. The methodology for processors is more complex. The test can be [BRY98] :

- *Dynamic* - actively exercise a DUT during beam exposure while counting errors, generally by comparing DUT output with a reference device or other expected output. Devices may have several dynamic test modes, such as *Read/Write* or *Program-Only*, depending on their function. Clock speeds may also affect SEE results.
- *Static* - load device prior to beam irradiation, then retrieve data post-run, counting errors. In this case there is the worst case estimation of the error rate.
- *Biased (SEL only)* - DUT is biased and clocked while I_{CC} (power consumption) is monitored for latch-up or other destructive conditions.

Electronic test equipment for controlling and observing the DUT behavior during its exposition to radiation must be built according to the system and the radiation facility.

4.1.1 THESIC Test System

An example of electronic test equipment for ground test facilities is THESIC system (Testbed for Harsh Environment Studies on Integrated Circuits) developed at TIMA laboratory [VEL98].

THESIC is a platform for SEU ground testing and fault injection purposes. It is organized in two boards, a motherboard for control of testing operation under radiation and user interface with a PC, and a daughter board for the adaptation of the device under test (DUT) to the motherboard bus protocol. Figure 4.1 shows the schematic of THESIC.

The communication between the two boards is achieved in asynchronous way through a common memory, called MMI (Memory Mapped Interface). Typically, during a test the DUT indicates by an interruption when the MMI area has data to be transferred to motherboard. When this happens, the motherboard interrupts the DUT board to read the results and thus detect errors. To cope with critical errors (black out situations resulting of upsets affecting the program sequencing) a programmable software watchdog was implemented in the motherboard.

The Motherboard controls all the operations related with the DUT test such as power on/off, current consumption control, test stimulus download, starting /stopping test cycles; receiving, pre-processing and transmitting data to/from user interface computer, via a serial link (RS232).

The Daughter board implements a totally free architecture where the DUT (Device Under Test) will be exposed to environment effects while exercised by the chosen test stimulus. To cope with a wide range of different types, two modes were provided: (a) slave DUT mode, in which all test operations are performed by the motherboard, and (b) asynchronous master DUT mode, in which the daughter board has its own processor (under test or not). In both modes communication is achieved through a memory area resident in the daughter board and accessible to the motherboard.

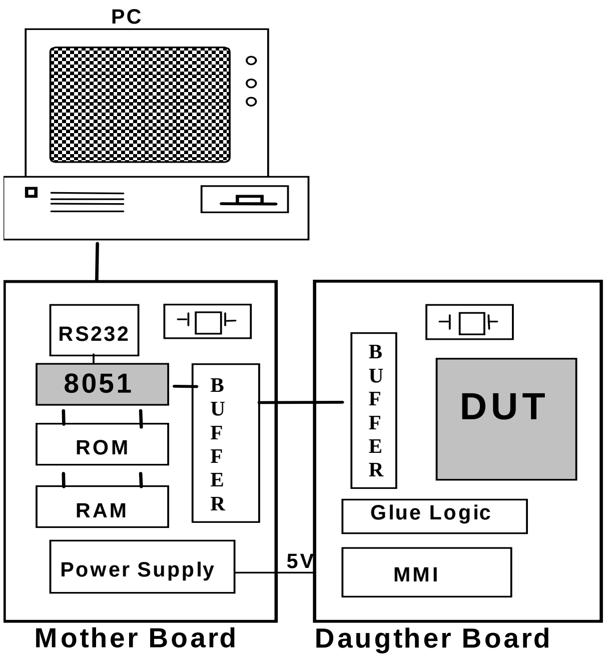


Figure 4.1 – THESIC schematic

When the circuit under test is a processor, errors perturbing test control operation may have consequences that are difficult to be predicted and/or understood through the analysis of corrupted data. As an example, transient errors affecting the program counter or the instruction register of a processor, may lead to sequence loss which could result in "black out" situations at the motherboard level. To cope with such critical errors, a programmable software watchdog was implemented in the motherboard.

The capabilities of THESIC tester were widely proved during lastly performed test campaigns, which aimed at the evaluation of the operation under radiation of various parts including two 64 KB SRAM's (from Hitachi and Matra Harris Semiconductors), general purpose microprocessors and micro-controllers (transmitter T225, 80C51) and dedicated co-processors (LNEURO 1.0 neural circuit from Philips Labs., WARP 2.0 fuzzy controller from SGS-Thomson). Detailed results of these tests can be found in [VEL98]. Figure 4.2 shows the THESIC hardware within the vacuum chambers available at the cyclotron 88" of LBL (Lawrence Berkeley Laboratory) facility. The motherboard shown in the background is fixed to a moving stage support allowing performing the alignment DUT-beam. It communicates to an external PC through a serial link connection. During a radiation test, target DUTs included on a daughter board is successively aligned with the beam.

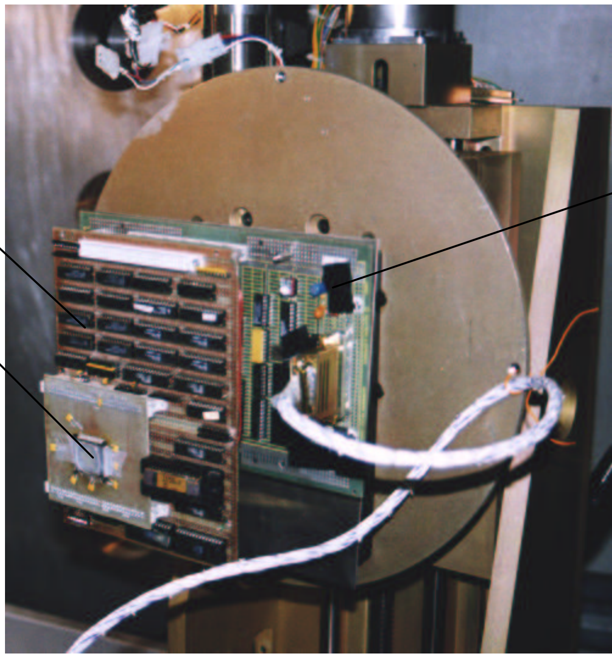


Figure 4.2 – THESIC system within the vacuum chamber available at LBL (Berkeley-California) facility.

4.2 Space projects

In the first type of test, the devices may be included in space projects (space stations, scientific satellites, etc) to get objective data about the behavior in space. Current radiation effects models are not sufficiently accurate to predict the radiation effects in new high-speed, low-power, high-density microelectronic devices, without validation from space results. To reduce risk, space testing of the sub-micron generation of devices is used in many applications because they are more accurate than ground testing and modeling programs. However, such long-term projects are practically reserved for space agencies.

An example of a space project is the Microelectronics and Photonics Test Bed (MPTB) [RIT99]. The purpose of this program is to perform radiation tests on identical devices (same lot, batch and wafer) and to compare to various radiation ground test facilities for each device type or subsystem to be flown. The devices are modeled and predictions of their radiation degradation and upset rates in space are made in advance of launch based on current NASA and CNRES (French Space Agency) radiation environment models for the radiation belts, cosmic rays and solar flares. The Microelectronics and Photonics Test Bed (MPTB) has been in space since beginning 1998 and it will be operated on-orbit over a period of four years. It will be able to assess the effects of natural radiation on the function and performance of a variety of state-of-the-art and "cutting edge" semiconductor and photonic devices and components.

Others examples of space agencies projects are:

- STVR (Scientific and Technologic Research Vehicle) from DERA UK (Defense Research Agency). Ariane 5 launched STRV on April 2000. The TIMA laboratory /NASA experiment is devoted to provide data about the SEE sensitivity of various FPGAs and the intrinsic robustness of digital implementations of fuzzy logic controllers.
- OTTI (Orbital Technologic Testbed Instrument), from NASA and NRL, is under study for a launch in 2001. A TIMA laboratory /CNES (French Space Agency) experiment is in the design phase. It integrates sub-micron circuits including different SEU hardened memory cells.
- CESAR project is an Earth Observation Satellite Mission developed in cooperation between INTA (National Institute for the Aerospace Technique, Spain) and CONAE (National Commission for Space Activities, Argentina). [REZ00]

4.3 Radiation Ground Test

The second type of test is the radiation ground test. It consists in exposing a circuit, while it carries out a given activity, to an appropriate particle beam. Such on-line testing needs:

- a particle beam,
- a test methodology, defining the activity of the device under test (DUT),

- an electronic test equipment for controlling and observing the behavior of the DUT during its exposition to radiation.

The goal of SEU testing is to determine the cross section vs. LET curve by irradiating the device being tested with different species of particles, at various angles, to render a range of effective LETs.

The particle beam can be obtained by Radiation Facilities such as particle accelerators: cyclotron, linear accelerators and synchrotron equipment based on fission decay sources such as Cf^{252}. Figure 4.3 exemplifies a radiation facility from Berkeley [http://www.aero.org/seet/primer/SEEtesting.html].

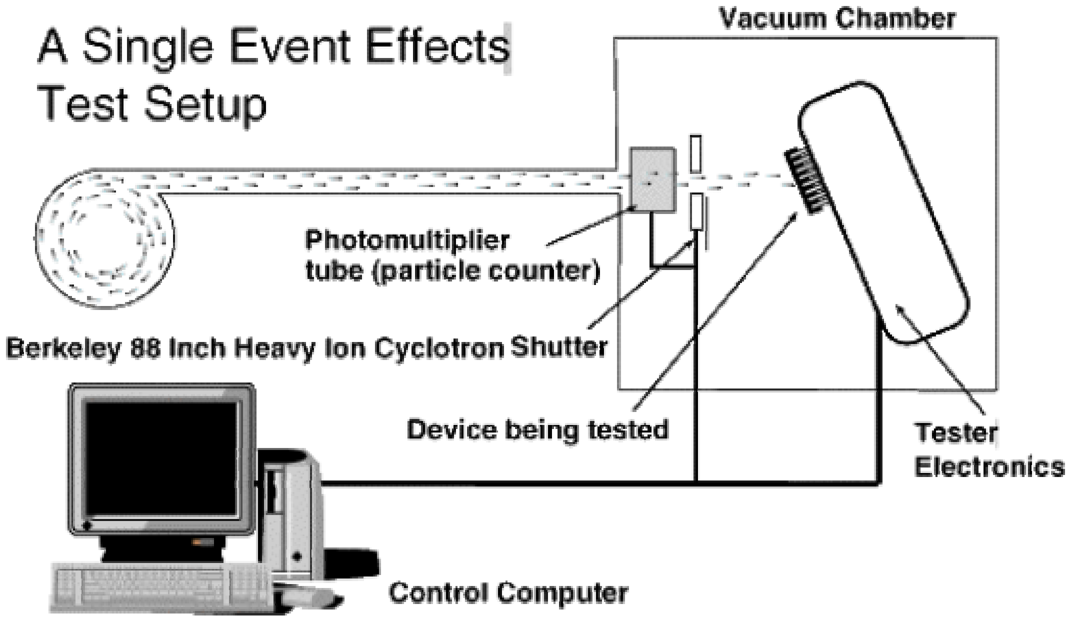


Figure 4.3 – Radiation Facility from Berkeley for ground testing of ICs

Examples of Radiation Facilities are: Brookhaven National Laboratory SEUTF (BNL - heavy ion), Lawrence Berkeley Labs 88" Cyclotron (LBL - heavy ion), Texas A & M University Cyclotron (TAMU - heavy ion), Paul Scherrer Institute (PSI - proton), Michigan State University National Super Conducting Cyclotron Laboratory (MSU - heavy ion and proton), University of California at Davis Crocker Nuclear Lab (UCD - proton) and Indiana University Cyclotron (IU - proton).

Figure 4.4 shows an experimental cave at the 88' cyclotron of LBL (Lawrence Berkeley Labs) devoted to SEE testing with heavy ions.

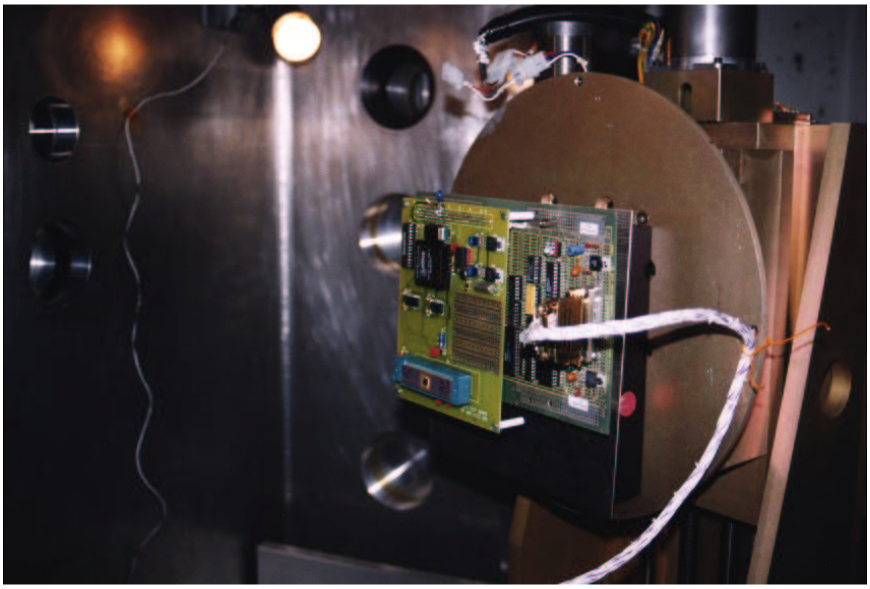


Figure 4.4 – Radiation facility from Berkeley

Energetic atoms ranging in atomic number from 1 (hydrogen) to 26 (iron) and beyond are primarily responsible by SEUs. Table 4.1 shows examples of heavy ions used by the Van De Graaff accelerator in Brookhaven National Laboratory (BNL).

Table 4.1 – Test Heavy Ions

ION	Energy (MeV)	LET (Mev*cm2/mg)	Range in Si (μm)
Cl-35	210	11.4	63.5
Ti-48	227	18.8	47.5
Ni-58	278	26.2	41.9
Br-79	286	37.2	39
I-127	320	59.7	34
Au-197	350	82.3	27.9

Where: LET (Linear Energy Transfer) is the energy absorbed by the target through which a particle is traveling per unit length of the track of the particle. For the purposes of this calculator, the LET is expressed in units of MeV/mg/cm2 (Million electron volts per milligram per square centimeter).
Range: the distance a particle of a given energy will travel through the target until it is stopped. For the purposes of this calculator, the Range is expressed in microns.

The range of energies and corresponding LET values achievable for a few representative beams are shown in figure 4.5. Many other ions are available and, up to date, about 35 different elements have been accelerated in Brookhaven Single Event Upset Test Facility.

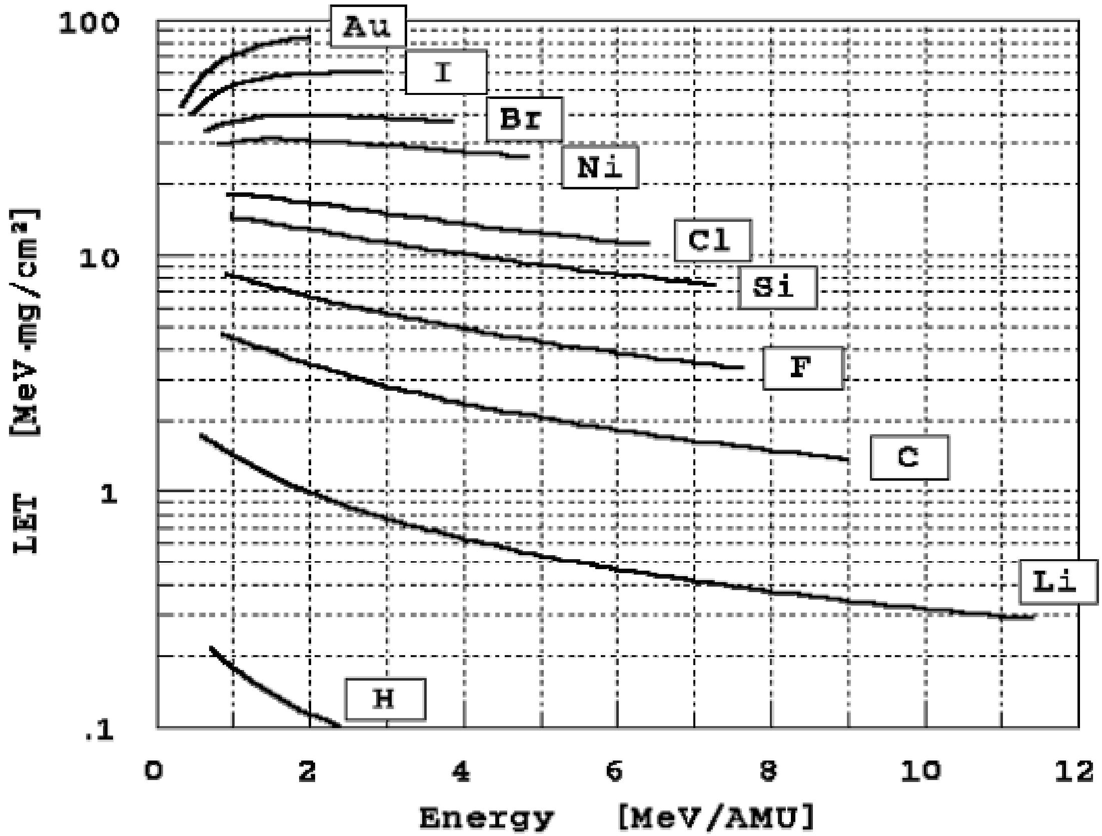


Figure 4.5 – Beam energies and corresponding LET values in silicon for a few representative beams available at the Brookhaven Single Event Upset test facility.

4.4 Fault Injection

The fault injection methodology is a way to test electronic circuits inside laboratories without using electron beams. The fault injection results can help research decisions reducing the cost and the turnaround time of underground tests.

This approach consists on the injection of bit flips, randomly in time and location, concurrently with the execution of a program. This can be achieved with minimal "intrusiveness" by software/hardware means, using the interruption mechanism. This method is presented in [VEL00] and [REZ00] and it uses the THESIC platform. This method supposes that the tested application is a processor-based electronic board, organized around a device capable to execute instruction sequences and to take into account asynchronous signals (interruptions). The key idea is the generation and storage at an appropriate memory address, of a piece of code, called here *CEU (Code Emulating an Upset),* whose execution will provoke the inversion content of the selected bit, called *CEU target*. If the processor is properly configured the CEU-code execution can be triggered by the assertion of an interrupt-like signal. The interruption activation instant and the CEU-target can be pseudo-randomly chosen by an ad-hoc external mechanism. In this way, bit flips may be injected in all accessible processor’s CEU targets (internal registers and SRAM memory area) as well as in the external SRAM where program data and code is stored.

This approach also reaches critical registers such as program counter, stack pointer, status register, etc…. It is important to note that the CEU code may include instruction sequences to read, modify and overwrite, values stored in the stack. This makes possible to inject CEUs on PC and other context registers, sometimes not directly accessible by the instruction set.

Advantages of the fault injection strategy are reducing test costs, turnaround time for research proposes, the possibilities of automation using flexible models in terms that several modules can be migrated on tests developed for other processors. Nevertheless, it must be mentioned two limitations of the CEU injection approach: as interruptions are always taken into account at predetermined fixed instants, the effects of SEUs occurring during instruction execution are not possible to be simulated, not all possible upset sensitive targets can be upset. However, due to the fact that the internal memory in the actual processors occupies a huge percentage of the processor area, the internal memory represents an accessible representative area of the total sensitive area. This gives significant results using the fault injection approach.

5 Single Event Upset Mitigation Solutions

Total ionization dose (T.I.D.) effects and single event latch-up (S.E.L.) can be reduced to acceptable levels using some of the existing CMOS technologies, for example the Epi-bulk CMOS process. However Single Event Upsets (S.E.U.s) represent radiation induced hazards, which are more difficult to avoid in the space applications especially in high-density sub-micron integrated circuits.

A SEU immune circuit may be fulfilled through a variety of mitigation techniques, including hardware, software, and device tolerance solutions. The most cost efficient approach may be an appropriate combination of SEU-hard devices and other mitigation solutions. However, the availability, power, volume, and performance of radiation-hardened devices may difficult their use as mentioned before. Hardware or software design also serves as effective mitigation, but design complexity may be a problem. A combination of the two may be a good select option.

Solutions to turn a logic device SEU tolerant can be implemented at different steps of the device development process. The mitigation solution can be divided in:

5.1) *Hardening by technology*, where an specific technology process for fabrication is used,

5.2) *Hardening by design*, where logic structures are modified to achieve the SEU immunity,

5.3) *Hardening by system*, where modifications in the software and duplication in the logic modules are performed.

5.1 Hardening by Technology

When particles hit the silicon part, they can affect the device in many different ways according to the technology process. Figure 5.1 illustrates three examples of a particle hitting a standard CMOS device, an epitaxial CMOS (Epi-bulk) device and a Silicon-on-insulator (SOI) device.

The standard CMOS process does not eliminate SEL and SEUs. Epi-bulk CMOS process is very efficient for SEL but it does not eliminate SEUs. Silicon on Insulator (SOI) process practically eliminates SEEs.

The SEU mitigation technique by technology consists in the use a specific technology process to turn the entire device immune to radiation particles such as Silicon on Insulator CMOS process. In this case the charged particle has much less chance to affect the device. The next subsection explains this technology in more details.

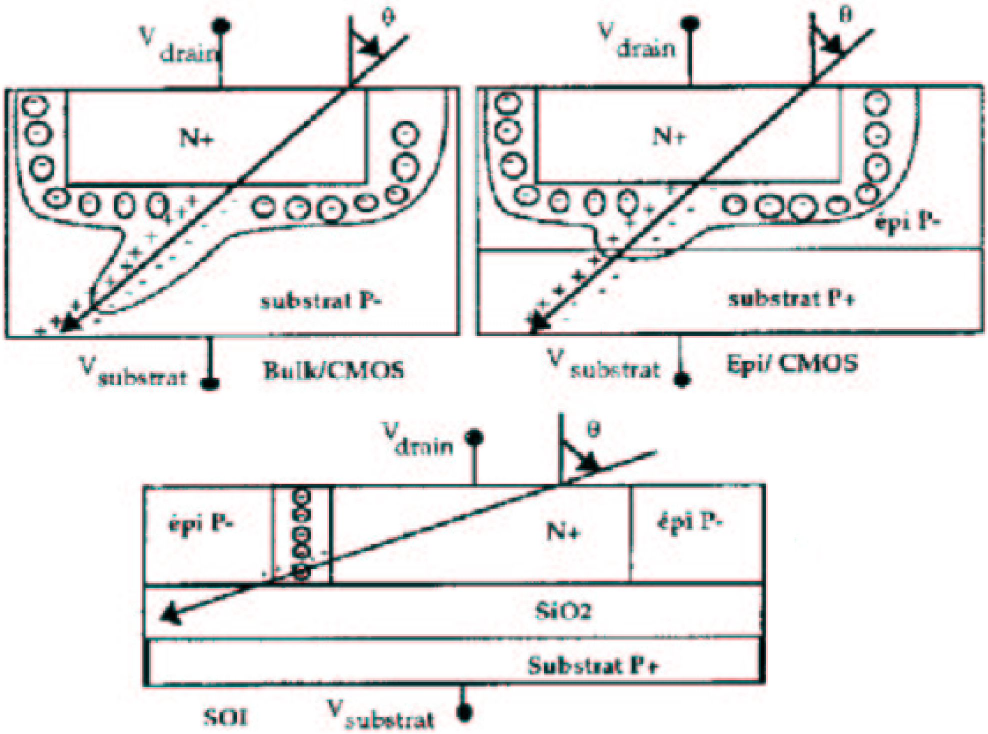


Figure 5.1 – The charge effects into different technology process

5.1.1 Silicon-on-insulator (SOI) technology process

Silicon on Insulator (SOI) technology [IBM00] is characterized by the placement of a thin layer of silicon on the top of an insulator during the chip manufacturing process. It helps to improve the performance of the chip. The transistors are then built on top of this thin layer reducing thus the capacitance. The isolation of each transistor makes SOI technology latch-up free. This thin layer of silicon on top of the insulator also helps to protect the bulk from charged particles, reducing the SEU effect.

SOI has been under active consideration for the last 30 years because of its high cost. However, nowadays due to its electric advantages researchers have started developing ways to implement this technology in a large fabrication process. Figure 5.2 illustrates the difference between standard CMOS technology process and SOI technology.

SOI technology improves performance over bulk CMOS technology by 25-35%, equivalent to two years of bulk CMOS improvements. SOI technology also has power consumption advantages of 1.7-3 times.

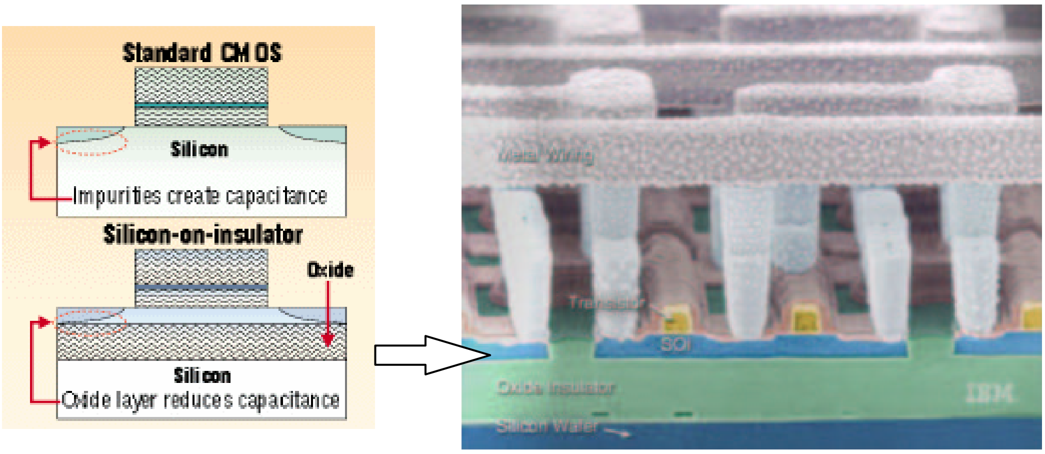


Figure 5.2 – Difference between standard CMOS and Silicon on Insulator (SOI)

The main drawback of this approach is the fabrication cost. Since the SOI technology is not already used for high volume circuits, the circuits fabricated in SOI process are expensive. This also eliminates the idea of using Commercial Of-The-Shelf (COTS) circuit technology.

"There are some inherent challenges in implementing SOI technology, but we have made significant progress on all those fronts at IBM. Initially there is always some resistance to new technologies within the semiconductor industry, but once people see it is the best way to solve a problem they become willing to use it. The industry will move to SOI technology. It is just a matter of time", said Bijan Davari, IBM (02/17/99) [http://www.techweb.com].

5.2 Hardening by Design

The design level solution is very attractive because it lets the use of a standard CMOS process. However, this solution is specific for each kind of circuit. For example, a micro-controller or an ASIC can have different design techniques to avoid SEU. The design engineer is responsible to project the hardened circuit according to it architecture and application.

Representative techniques of SEU mitigation at design level solutions are:

5.2.1) Triple Modular Redundancy of the memory cells with voting (TMR),

5.2.2) Hardened gate resistor memory cells,

5.2.3) Hardened memory cell using feedback structures,

5.2.4) Hamming code and decode logic blocks.

5.2.1 Triplicate Modular Redundancy of Cells with Voter

This solution consists in the triplication of memory cells and to implement a voter to chose the correct stored value. This solution completely eliminates the risk of

SEU. However, the main drawback is the high number of transistors resulting in more than 4 times silicon area overhead. Figure 5.3 illustrates this approach.

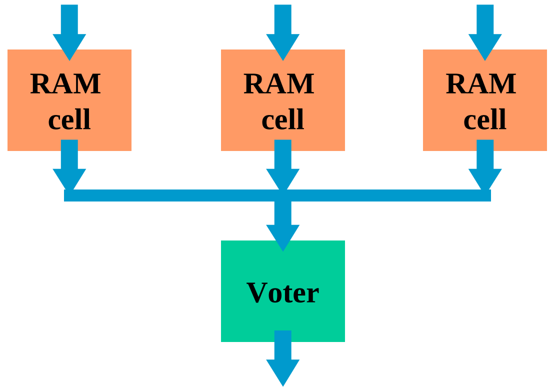


Figure 5.3 – Triple Modular Redundancy (TMR) solution

5.2.2 Hardened Gate Resistor Memory Cell

This solution uses a resistor gate to protect the memory cell data from SEUs [WEA87]. The gate resistor high resistance (off state) protects the stored cell data from a bit-flip. It provides a high silicon density. The decoupling resistor slows the regenerative feedback response of the cell, so the cell can discriminate between an upset causing voltage transient pulse and a real write signal. The gate resistor can be built using two levels of polysilicon. Figure 5.4 illustrates this approach.

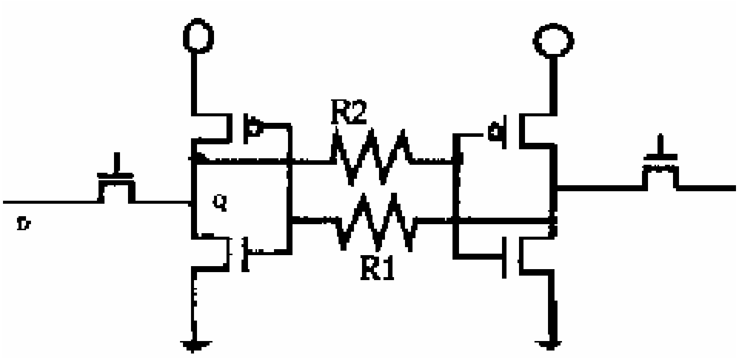


Figure 5.4 – SRAM cell based on gate resistor

An important characteristic of the gate resistor is that it has a little impact in the circuit density. The main drawbacks are temperature sensitive, performance vulnerability in low temperatures, and extra mask in the fabrication process.

5.2.3 Hardened CMOS Memory Cells composed of Feedback Structures

The main idea is to provide CMOS memory cells with an appropriate feedback devoted to restore the data when it is corrupted by an ion hit. The principle is to store the data in two different locations within the cell in such way that the corrupted part can be restored. The main problem is how to organize the extra transistors used to realize the feedback that will result in new sensitive nodes, without affecting the SEU sensitivity.

The main advantages of this method are high performance (read/write time), low sensibility to temperature, technology process independence and voltage supply good SEU immunity. The main drawback is silicon area overhead.

Many memory cells based on this approach have been developed in the last years. The section 6 gives details of some of them.

5.2.4 Hamming code and decode logic blocks

The idea of this SEU hardened technique is to identify that an error has occurred in a latch, flip-flop, register or memory and to correct the error when the stored value is used. It is necessary extra logic structures to correct the errors according to the amount and the class of stored cells located in the circuit.

Hamming Code is an error-detecting and error-correcting binary code that can detect all single- and double-bit errors and correct all single-bit errors. This coding method is recommended for systems with low probabilities of multiple errors in a single data structure (e.g., only a single bit in error in a byte of data).

Hamming Code Definition:

A Hamming code satisfies the relation $2^k >= m+k+1$, where $m+k$ is the total number of bits in the coded word, m is the number of information bits in the original word, and k is the number of check bits in the coded word. Following this equation the Hamming code can correct all single-bit errors on n-bit words and detect double-bit errors when an overall parity check bit is used. According to the number of check bits, it is possible to correct more than a single-bit error.

The check bits are placed in the coded word at positions 1, 2, 4, …, $2^{(k-1)}$. For example, for 8-bit data, 4 check bits (p1, p2, p3, p4) are necessary so that the Hamming code is able to correct a single-bit error. Figure 5.5 exemplifies a 12-bit coded word (m=8 and k=4) with the check bits p1, p2, p3 and p4 located at positions 1, 2, 4 and 8 respectively. The check bits are able to inform the position of the error.

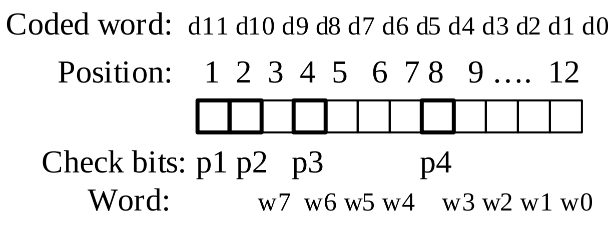


Figure 5.5 – Hamming code 12-bit word and the check bits

The check bit p1 creates even parity for the bit group {1, 3, 5, 7, 9, 11}. The check bit p2 creates even parity for the bit group {2, 3, 6, 7, 10, 11}. Similarly, p3 creates even parity for the bit group {4, 5, 6, 7, 12}. Finally, the check bit p4 creates even parity for the bit group {8, 9, 10, 11, 12}, as shown in figure 5.6.

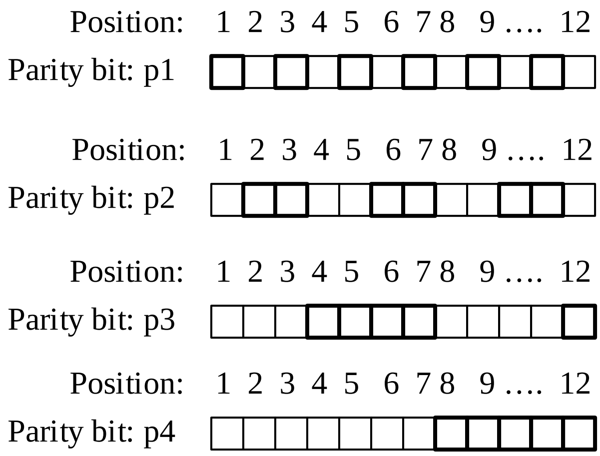


Figure 5.6 –Hamming code check bits generation

An example of SEU mitigation technique using Hamming Code is presented in [COT00], [LIM00]. This work presents a full radiation hardened version of 8051 micro-controller designed with a VHDL description protected by Hamming Code.

Micro-controllers operating in the space environment can be affected by SEU. Thus, the memory cells and registers included in microprocessors must be protected to avoid potential transient errors. The MSC8051 [INT98] VHDL description presented in [CARRO96, GILM97] was re-used to insert SEU radiation fault tolerant structures. The original code is entirely compatible with the INTEL 8051 microprocessor in terms of instruction timing. The microprocessor description is divided into six main blocks, illustrated in figure 5.8. These units are finite state machine, control unit, instruction unit, datapath and RAM and ROM memories.

The 8051 micro-controller described in VHDL has many registers in the control unit, state machine and datapath. Table 5.1 shows all these registers and the number of latches. The internal memory has 128 bytes which represent 1024 latches.

Table 5.1 – Sensitive Area of the 8051 micro-controller

8051 unit	# latches	Signal description
Control Unit	11	Latch_int0 (1 bit), Interrupt_state (2 bits), Instruction (8 bits)
State Machine	15	State (5 bits), Next_state (5 bits), Current_state (5 bits)
Datapath Unit	104	Alu input a – reg_a (8 bits), Alu input b – alu_2 (8 bits), Alu output – out_alu (8 bits), PC (8 bits), PC_2 (8 bits), SP (8 bits), ACCU (8 bits), Instruction (8 bits), InBus (8 bits), RAM output – dram_out (8 bits), RAM addr low – RamAd (8 bits), RAM addr high – dph (8 bits), ROM output – memo (8 bits)
Internal Memory	1024	Memory values (128 bytes)

In order to protect all the memory structures of the 8051 micro-controller by hamming code, 8 combinational components were described. The first group of 4 components receives a 1-bit, 2-bit, 5-bit or 8-bit data and returns a 3-bit, 5-bit, 9-bit or 12-bit coded word, respectively. The second group of 4 components receives a 12-bit, 9-bit, 5-bit or 3-bit word and returns an 8-bit, 5-bit, 2-bit or 1-bit decoded and corrected data. Figure 5.7 shows the schematic of the 8051 and the protected blocks in bold (control and finite state machine, datapath and internal memory).

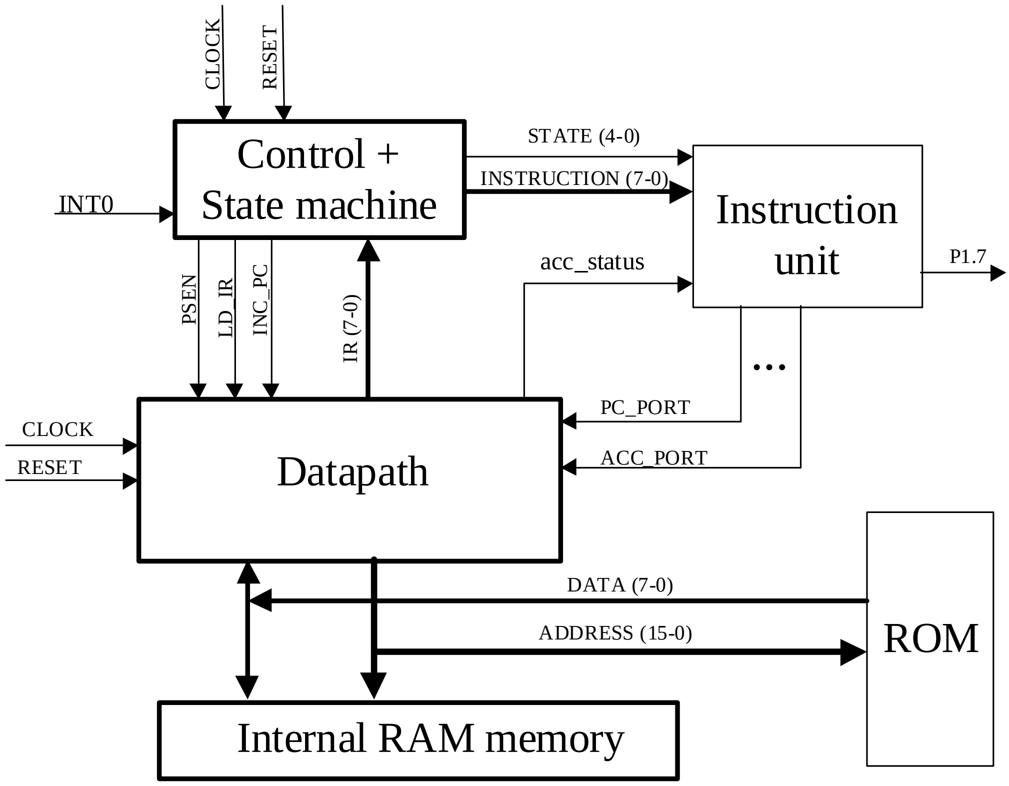


Figure 5.7 – General scheme of the SEU hardened 8051

The stored value is corrected each time that it is read by the hamming decodification. Figure 5.8 shows a Hamming Code protection in an 8-bit data using the Hamming Codification block and the Hamming Decodification block.

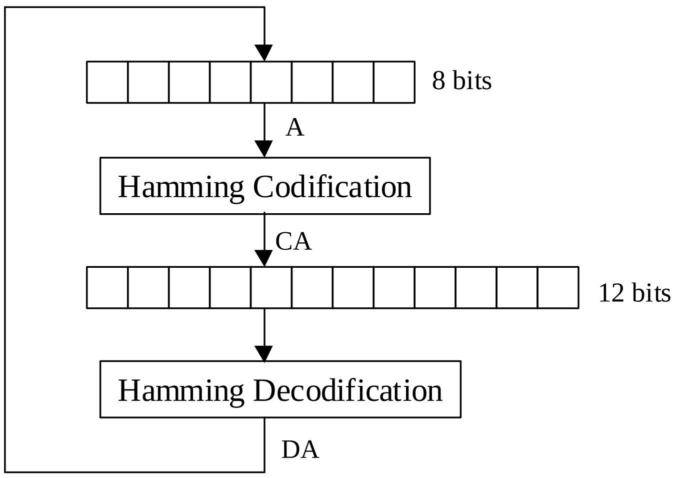


Figure 5.8 – Hamming Code protection schematic in an 8-bit word

5.3 Hardening by System

SEU mitigation techniques may also be performed at the system level. These techniques can be done in the software, for instance duplicating variables, or in the hardware system, by triple modular redundancy (TMR) of components, inserting some error detection and correction blocks used to rewrite or re-transmit the correct data or using watch dogs for microprocessor.

When performed in the software, the system level solutions permit the SEU mitigation without modifying the system structure. In this case it is completely COTS technology devices SEU immune. Consequently it presents all advantages in terms of cost, performance and data sheets.

5.3.1 Module and Device Redundancy

Redundancy between circuits, systems, etc., provides a potential means of recovery from a SEE on a system. Autonomous or ground controlled switching from a prime system to a redundant spare may be an option, depending on spacecraft power and weight restrictions. With three identical circuits, the voter can choose the output that at least two agree upon. Figure 5.9 exemplifies this approach.

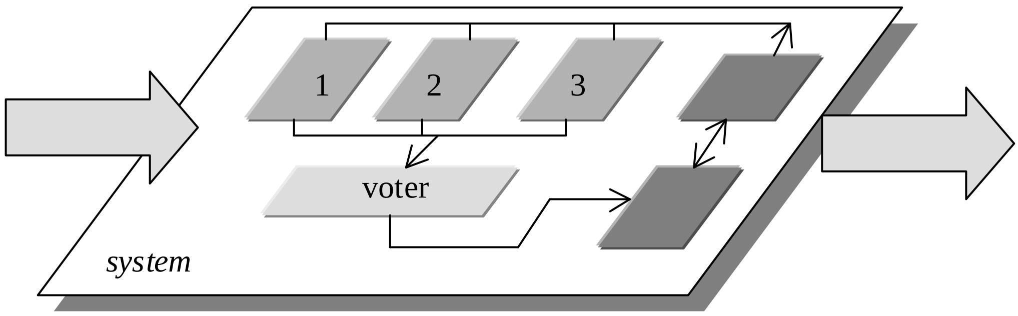


Figure 5.9 – Triplication of devices in a system

The main drawback of this technique is that the voter must be designed in such way that no error can occur in the voter. In this case, the voter is designed using some previous techniques in the circuit or design level.

5.3.2 Error Detection and Correction Solutions

The Error Detection and Correction (EDAC) solutions [LAB99] are examples of solutions that can be used to detect or/and correct SEUs when they occur. Some of them can achieve an acceptable level of reliability.

The first example of EDAC is parity checking. It is a "detect only" scheme, which counts the number of logic one states in a data set producing a single parity bit reporting whether an odd or even number of ones were count in that data. This scheme will flag an SEU error only if an odd number of bits are in error (multiple SEUs). Although this solution is largely used to detect errors in memories, it is not sufficient to make a SEU hardened memory because it can not correct an error. Figure 5.10 exemplifies the parity bit check in an 8-bit data.

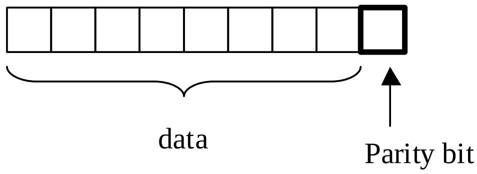


Figure 5.10 – Example of parity check in an 8-bit word

The second example is the Hamming Code technique. This approach can be used either in the circuit design or in the system level. Using Hamming code as a SEU mitigation solution in the design of a circuit, extra logic blocks are needed to code and decode the stored values such as registers and internal memory. This technique is very efficient and it was presented before in a SEU hardened micro-controller.

The hamming code can also be used in system level to code and decode variables in systems based on microprocessors. For example, a system composed of various integrated circuits including a microprocessor and memories can protected important variables using the hamming code. The code and decode implementation are performed in the assembler code described as sub-routines. The program runs in the microprocessor. Figure 5.11 exemplifies the hamming code technique running in a system board.

Although this approach can reduce dramatically the performance of the application, it does not require component changes in the board. Consequently, it is a low cost option and according to the system application, this level of reliability can be acceptable.

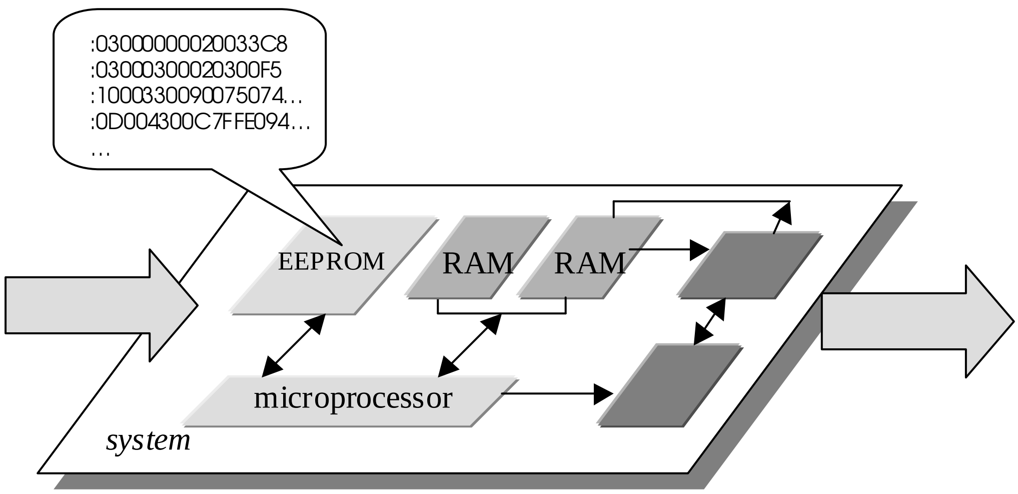


Figure 5.11 – Hamming code running in the Assembler of a system board

Another option to error correcting codes is the Reed-Solomon (R-S) coding [PLA00]. The R-S code is able to detect and to correct multiple and consecutive data errors. This method is used in the integrated circuits designed by the NASA VLSI

Design Center. Let there be *n* storage devices, *D0, D1,…, Dn*, each of which holds *k* bytes. These are called the "Data Devices". Let there be m more storage *devices C0, C1, …, Cm*, each of which also holds *k* bytes. These are called the "Checksum Devices." The contents of each checksum device will be calculated from the contents of the data devices. The goal is to define the calculation of each *Ci* such that if any *m* of *D0, D1, …, Dn, C0, C1, …, Cm* fail, then the contents of the failed devices can be reconstructed from the non-failed devices. The calculation of the contents of each checksum device *Ci* requires a function *Fi* applied to all the data devices. The contents of checksum devices *C1* and *C2* are computed by applying functions *F1* and *F2* respectively.

The convolution encoding is another EDAC method and it differs from Hamming Code by checking bits into the actual data stream rather than into word groups, known as scrubbing, is common among current solid-state recorders flying in space. This provides good immunity for mitigating isolated burst noise, and is particularly useful in communication systems or Field Programmable Gate Arrays programmed by bit streams.

The above methods provide ways of reducing the effective bit error rate of data storage areas such as solid-state recorders and communication paths or data interconnects. Table 5.2 summarizes a sample of EDAC methods for memory, cores and systems.

Table 5.2 – Sample EDAC for memory, cores and systems

EDAC Method	EDAC Capability
Parity	Single bit error detect
Hamming Code	Single bit correct, double bit detect
RS Code	Correct consecutive and multiple bytes in error
Convolution encoding	Corrects isolated burst noise in a communication stream
Overlying protocol	Specific to each system implementation

The above techniques can be used to protect integrated circuits in space applications. Each one of these techniques has different impacts in system area and performance. The designer can choose which one is the more indicate method for each circuit and application. A combination of EDAC techniques may be more effective.

For high reliability systems it is recommended not only to use hardened devices based on the design techniques presented previously but also to use some systems protection such as watchdogs, etc…

6 CMOS SEU Hardened Memory Cells

Different kind of circuits like microprocessors, memories, ASICs, programmable circuits and others can be protected to SEU replacing the memory cells by the hardened cells presented in this section. Studies in this approach must report the main area and performance overhead of using hardened cells instead of the normal memory cell.

The basic idea of SEU hardened memory cells is to add elements in a standard memory cell with an appropriated feedback devoted to restore the data corrupted by an ion hit. The SEU immunity of these memory cells must be independent of processing, voltage supply and temperature tolerances.

Figure 6.1 presents three different standard memory cells without SEU tolerant mechanisms [RAB96]. The cells 4.1a, 4.1b, 4.1c have 4, 5 and 6 transistors, respectively. The cell 4.1b is used in Xilinx FPGAs but the most commonly used, as RAM cell is the 4.1c. The pass transistor is used to write and read the data to/from the cell. During the normal operation of the cell this pass transistor is turned off and the cell holds its value.

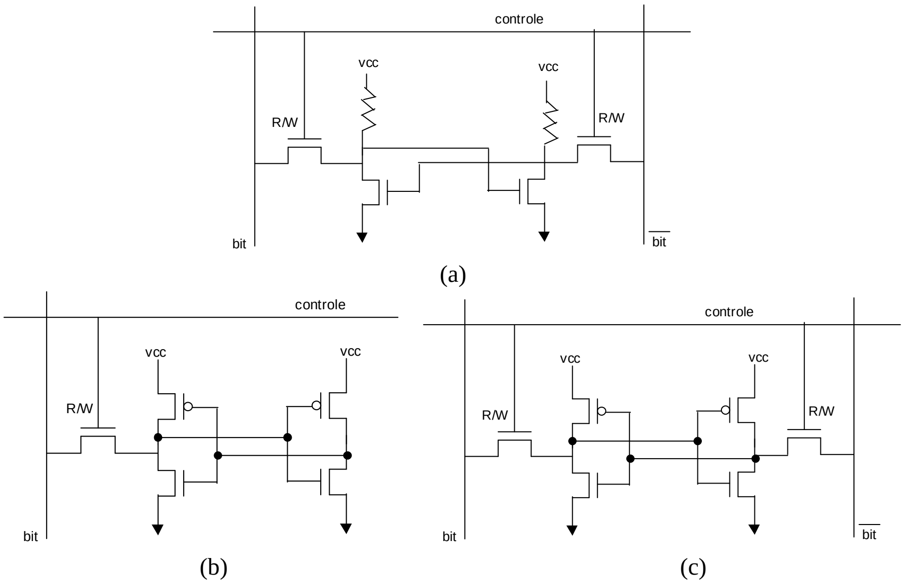


Figure 6.1 – Basic RAM memories cells

The 6 transistors memory cell that is largely used in CMOS circuits uses the data bit in both polarities providing a fast read and write with the increase of one transistor. The 4 transistors memory cell is used in high-density RAM memories. This cell has resistance (a few giga-ohms) between the transistors and V_{dd} increasing the transient error sensitivity.

In the last 10 years some designs hardened memory elements have been developed [BES93, CAL96b, LIU92, WHI91, WIS93]. In the next subsections some of these memory cells will be presented. All of them are based on duplication and feedback approaches. One differs from each other in terms of the number of transistors, performance and SEU immunity degrees.

Charged particle affects the memory cells inducing a current pulse in the drain of OFF transistors and it can flip the memory data, as it is presented in figure 6.2. Memory cell elements are very SEU susceptible because there are always two opposite transistors OFF that can be affected by a charged particle.

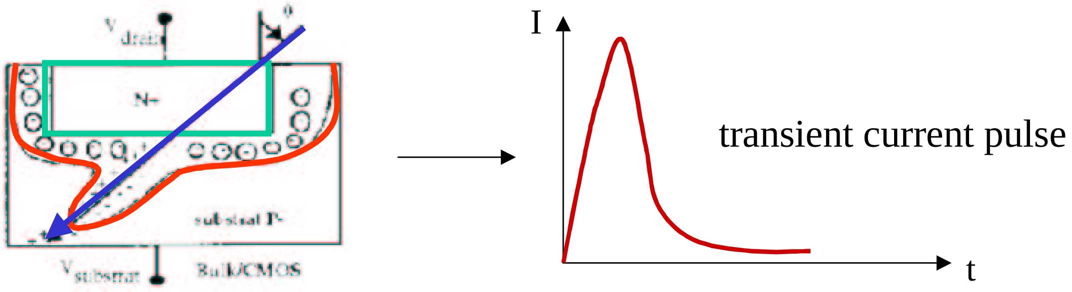


Figure 6.2 – Charged particle hitting the drain of an OFF transistor

Figure 6.3 shows the scheme of a typical 6-transistor memory cell that can be affected by a charged particle. In case of input D values "0", the transistors P2 and N1 are ON and transistors P1 and N2 are OFF. If a charged particle hits the drain of transistor P1 or N2, the transistor which its gate is connected to the upset drain will start to conduce. For example if P1 is upset by a charged particle, N2 turns ON and the node A will be "1" unless than "0" (initial value). In some instants, the memory value is flipped.

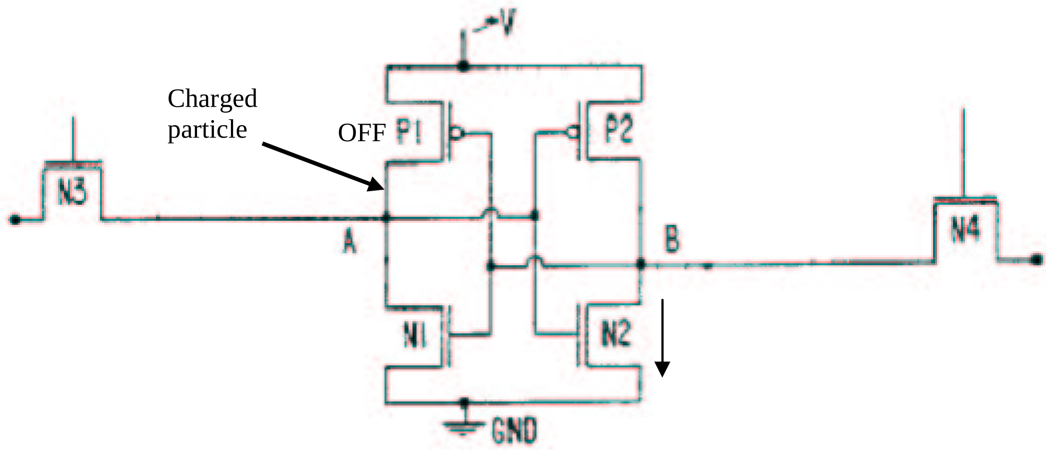


Figure 6.3 – A basic memory cell affected by a charged particle

6.1 IBM Memory Cell

A first design hardened memory cell was first proposed by IBM in a standard CMOS technology process in [ROC92]. It is composed of 6 transistors to build the memory part and 6 more p-channel transistors to provide SEU immunity capabilities to the latch. The figure 6.4 shows its transistor diagram.

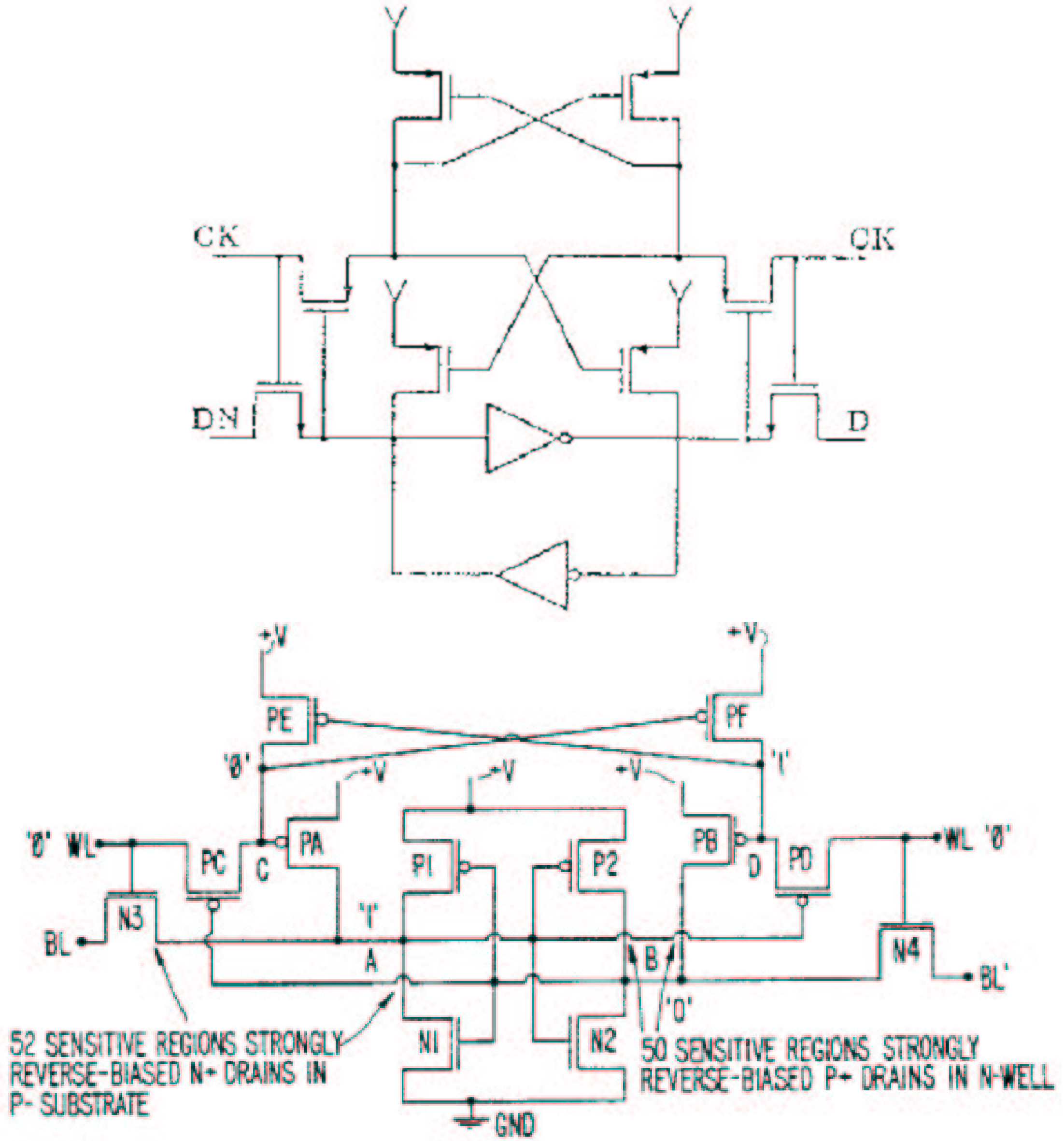


Figure 6.4 – IBM SEU immune memory cell

The transistors PA and PB are called data state control transistor, PC and PD are pass-transistors and PE and PF are cross-coupled transistors. The sensitive nodes are A, B, and C.

When a particle hits the node A, it instantly goes low and momentarily the cell is unstable with both nodes A and B at a relative low potential. Transistor PD momentarily turns on but node D cannot charge low enough to turn PB fully ON since transistor PF remains ON. However the presence of the fully ON PA transistor, reinforcing the pre-hit relatively positive data state at node A, restores node A without logic upset.

Considering now a particle hit occurring at node B, when the hit occurs node B instantaneously goes high turning transistor PC OFF, momentarily isolating the node C at its relative low potential. With the gate of transistors P1 and N1 connected to node B, the resulting data feedback response causes node A to attempt to go low. However, with the transistor PA ON reinforcing the preexisting high state in node A, node A maintain its high state data. Therefore node B eventually returns to its pre-hit low potential after the momentary disturbed condition, the transistor N2 once again pulls down node B. Thus node B recovers the logic upset.

Finally, if a particle hits node C, transistors PA and PF turn off momentarily. With respect to data information stored in the data cell, no harm is done and node C is eventually recharged low through the ON PC transistor. Node C recovers and there is no threat posed to the stored data.

Advantages of this cell are low static power dissipation and good SEU immunity. Some drawbacks of the implementation are the large number of transistors (there are16) and the size of transistors.

Experimental results with a prototype implementing a shift register using this latch cell show that no errors were detected for particles having a LET up to 74 MeV*cm^2/mg. This means that the LET_{th} for this cell is 74 MeV*cm^2/mg (table 2.1, section 2).

6.2 NASA Memory Cell I

This immune logic cell, also called Whitaker memory cell, is based on three fundamental concepts [WHI91]. First, the information must be stored in two different places. This provides a redundancy and maintains a source of uncorrupted data after a SEU. Second, feedback from non-uncorrupted location of the stored data must cause the lost data to recover after a particle strike. Finally, the current induced by a particle must flows from the n-type diffusion to p-type diffusion.

If a single type of transistor is used to create a memory cell then p-transistors storing a 1 cannot be upset and n-transistors storing a 0 cannot be upset. Figure 6.5 presents this cell. The concepts described above are applicable to the design of critical portions of any logic circuit.

This memory cell has 16 transistors and it is organized in two parts. The top half part is composed of only p-channel transistors and the bottom half part has only n-channel transistors. The transistors M2 and M4 are sized to be weak comparing to M3 and M5 while M13 and M15 are sized to be weak comparing to M12 and M14. The weak transistor sizes are approximately 1/3 of the normal transistor sizes. The size of the weak feedback transistors is responsible for the recovery time.

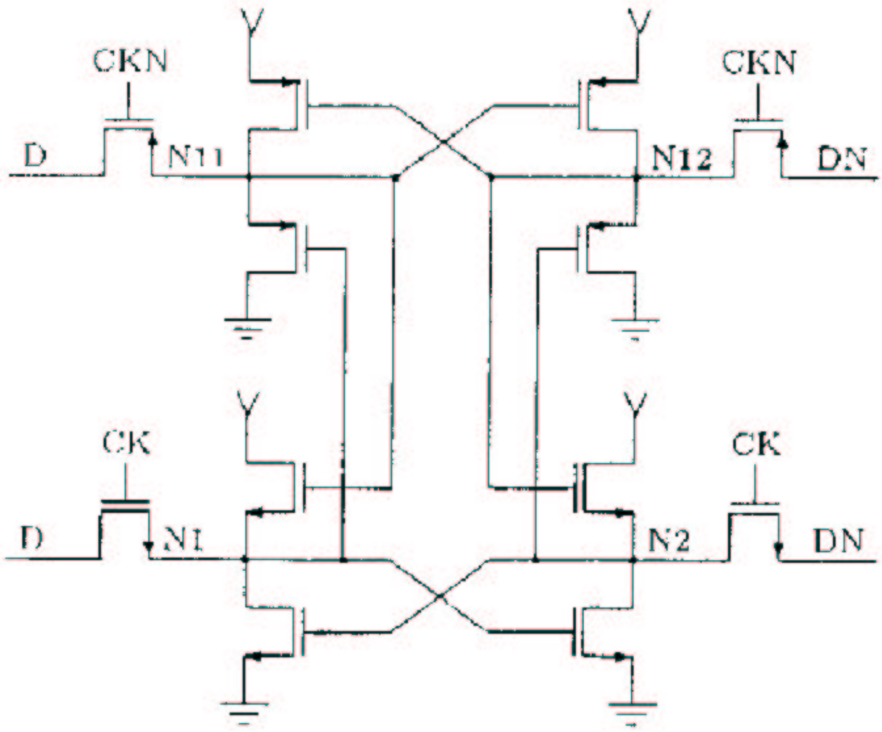


Figure 6.5 – NASA SEU immune memory cell

Nodes N1 and N2 can store 0's that cannot be upset and nodes N11 and N12 can store 1's that cannot be upset. If N11 is storing a 0 and a hit drives the node to 1, M14 turns off but N12 remains at 1. M2 turns on but is weak and cannot overdrive N1 keeping M13 on and restoring N11 to a 0. If N1 is storing a 1 and a particle hit drives the node to 0, M5 turns off leaving N2 at a 0. M13 turns on but it is weak and cannot over drive N11 keeping M2 on and restoring N1 to a 1. However the 0 level in node N11 and the level 1 in node N1 are degraded because the main principle of CMOS pass transistors. The internal voltage level reduces the noise margin.

The advantage of this approach is that transistors do not need to be designed in special sizes. One of the drawbacks of this cell is the high static power dissipation. The weak devices are not driven to cut off by the degraded levels and there is a ratio situation that results in static current between V_{dd} and V_{ss}. Tests were done using this cell in shift registers fabricated in a standard CMOS process. No disruptions in shift register functionality were observed for particles having LET up to 120 $MeV.cm^2/mg$.

6.3 NASA Memory Cell II

This cell is an improvement of the Whitaker's SEU hardened CMOS memory cell [LIU92]. This development has eliminated the static power consumption, reduced the number of transistors and eliminated the possibility of capturing an upset state in the slave section during a clock transaction.

The memory cell, presented in figure 6.6, consists in two storage structures. Complementary transistors M6/M7 (M16/M17) have been inserted between the power supply V_{dd} (V_{ss}) and n-type (p-type) memory structures. These transistors do not affect the SEU immunity of the memory cell. The DC path in this cell can thus be disconnected, eliminating power consumption.

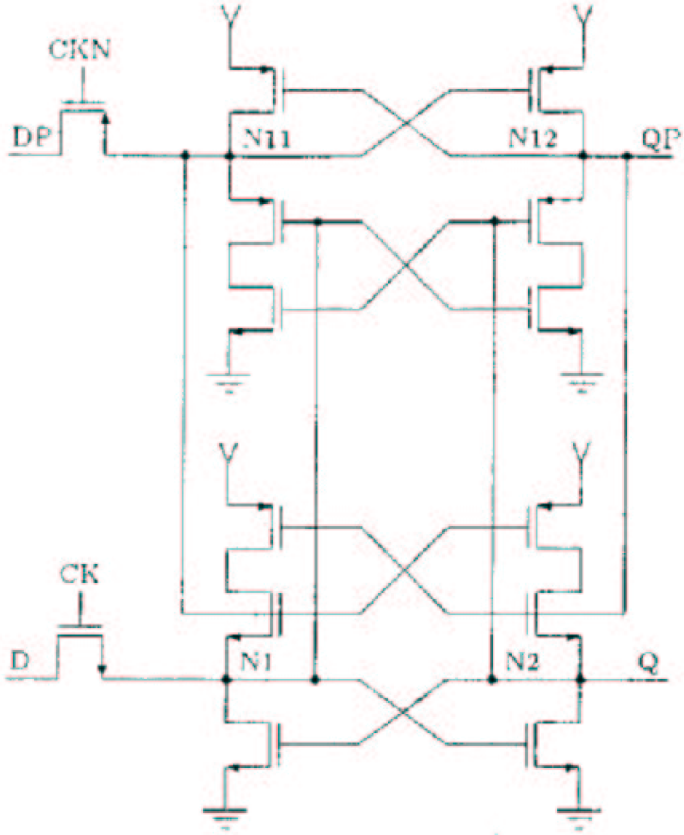


Figure 6.6 – Liu SEU immune memory cell

The n-transistors (M16 or M17) in p-channel memory is turned on during operation only if the output N11/N12 needs to be pulled to a 0. At that time, a 0 will be presented in both source and drain areas. A particle hit on a n-diffusion will not upset the 0 level. When the output N11/N12 is high both the n-transistors and p-transistors M16/M13 or M17/M15 are off and an upset in an intermediate node will not affect the output node N11/N12. Note that there are only two pass transistors in the RAM cell comparing with four in the previous design.

Tests were done utilizing this cell in shift registers fabricated in a standard CMOS process. No disruptions in shift register functionality were observed below to 30 MeV.cm^2/mg. However above 30 MeV.cm^2/mg the test chip latched up.

6.4 Canaris Memory Cell

This approach consists of building a memory cell from gates of an SEU-immune CMOS logic family [WIS93]. Figure 6.7 illustrates a memory cell implemented with And-nor and Or-nand gates.

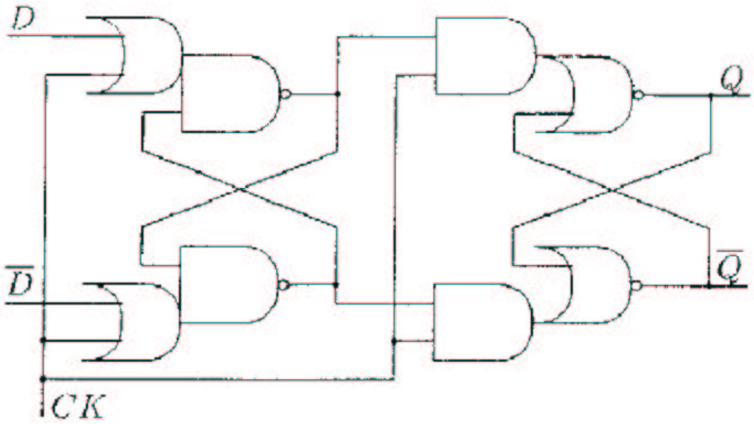


Figure 6.7 – Flip-flop implementation using or-nands and and-nors

The idea is to add two transistors per gate leading to a two-output logic gate. The gate consists in two transistor networks, p-channel network and a n-channel network. The gate has two outputs, Pout and Nout. One of these outputs will be used to drive P-channel transistors, while the other will drive N-channel transistors. Node Pout can provide a source of 1's which cannot be upset and node Nout provides a source of 0's which cannot be upset. Figure 6.8 shows the transistor level logic diagram of the SEU immune And-nor and Or-nand gates.

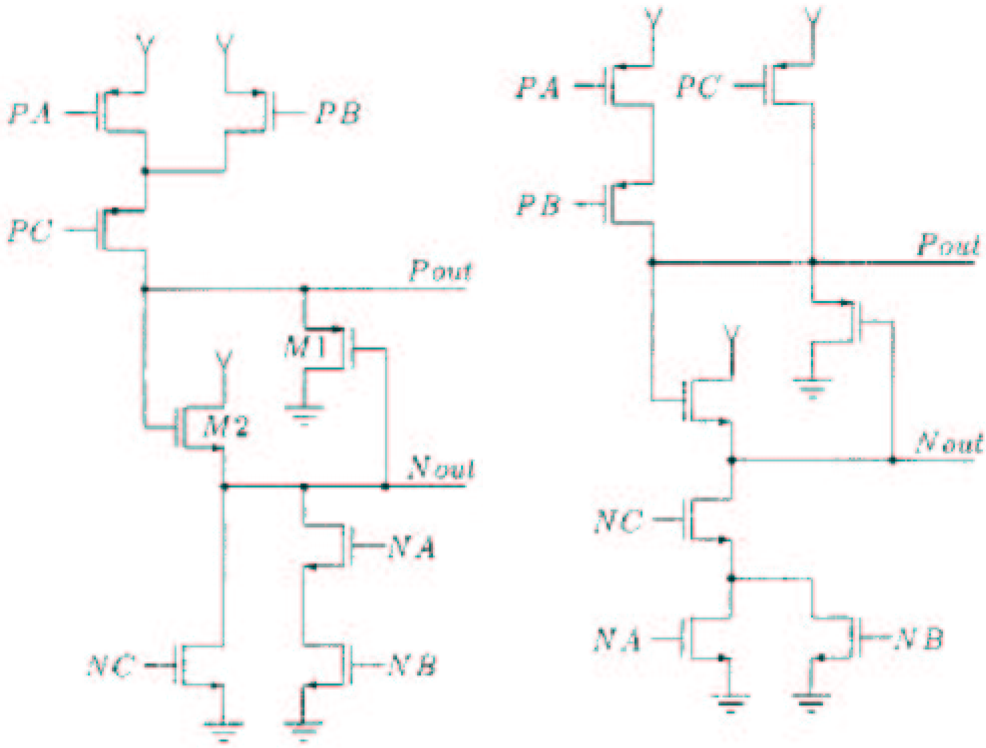


Figure 6.8 – Or-nand and and-nor SEU immune implementations

Transistor M1 is sized to be weak compared to the p-channel array and transistor M2 is sized to be weak compared to the n-channel array. The SEU immune mechanism works as follows. When the inputs are such that Pout and Nout are at a 1, only the Nout can be corrupted by an upset. If Nout is hit, driving the node to 0, the transistor M1 will turn on but it will not overdrive the p-array. Pout will remain at 1, transistor M2 will remain on, pulling the Nout back to 1. Conversely, if the inputs are such that Pout and Nout are at a 0, only the Pout can be corrupted by an upset. If Pout is hit, driving the node to 1, the transistor M2 will turn on but being week comparing to the n-array, Nout will remain pulled down to 0. Such a logic family can provide immunity of an upset event as well as recovery from the upset. A flip-flop implemented using these gates has 16 transistors and a master-slave flip-flop has 32 transistors using this approach.

This solution can be applied even for the combinational and sequential logic when memory cells are implemented using the SEU immune combinational gates. Using this approach all the combinational part of the circuit can be grouped in complex logic functions where each one of these functions has two extras transistors dividing their outputs. For large complex logic gates, two extra transistors may not represent a high addition of area. However, due to the duplications of outputs the number of internal connections can increase according to the implementation architecture (standard cells, gate arrays, FPGAs…)

There are some drawbacks using this solution for memory cells such as long recovery time after upset and leakage current problems that can appear due to total dose effects (parallel arrays of N-channel transistors are to be avoided). However, a prototype implementing shift-registers built from master-slave flip-flops designed using such gates has been presented in [WIS93] featuring excellent SEU immunity (no errors were detected for particles having LET up to 120 $Mev/mg/cm^2$).

6.5 HIT memory cells

Two new SEU-tolerant memory cells, called HIT (Heavy Ion Tolerant) cells have been proposed in [BES93], [VEL94]. These cells are composed of 12 transistors organized as two storage structures interconnected by feedback paths.

Figure 6.9 presents the HIT1 cell. In the normal operation**,** if the read/write signal is low (inactive) transistors MP1, MP4, MN2, MN6 and MP5 are ON, the other transistors being OFF. Then, it is easy to show that the logical states of nodes Q and Q' are conserved. Furthermore, as there are no direct paths from V_{dd} to V_{ss}, the stability of the HIT1 cell memorization function is guaranteed.

Read operation is performed by pre-charging to VDD data lines D and D'. As the read/write signal goes high, Q will remain at 1 because it is directly connected to the data line D through transistors MN1 and MN3. Node Q' will remain at 0 because MN4 and MN6 are both ON discharging data line D'.

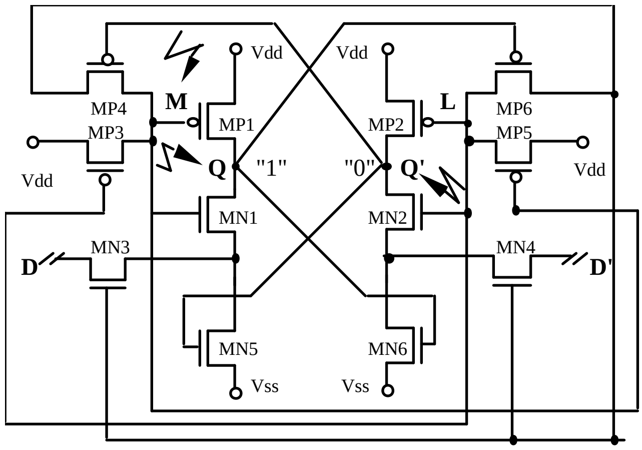


Figure 6.9 – The HIT1 memory cell

To modify the state of the HIT1 cell, the read/write signal should go high while the new values 0 and 1 are presented respectively at inputs D and D'. Then, P-channel transistor MP4 will push high node M turning respectively OFF and ON transistors MP1 and MN1. As transistor MN5 is OFF, Q is directly relayed to input D, forcing Q at 0. MN6 is turned OFF connecting directly output Q' to input D'. Q' is forced to 1, turning ON transistor MN5 and turning OFF transistor MP4, then asserting node Q to 0 and leading node M to high impedance.

The HIT1 cell has 3 sensitive nodes that are Q, Q' and M. The HIT1 cell behaviors for each node SEU effect are described in next paragraph.

If a particle strikes the drain of transistor MN1, node Q will go low. Transistors MN6 and MP6 will turn OFF and ON respectively. Then, node Q' is not biased but conserves its low state by capacitive effect. Transistors MP6 and MP5 are both ON but, as the width of MP5 is chosen larger than the width of MP6, node L will remain at 1. As transistor MP1 is still ON, node Q will be restored to 1, recovering the upset.

If a particle strikes the drain of the transistor MP2, node Q' will go to 1, turning transistors MN5 and MP4 respectively ON and OFF. Node M goes to high impedance, conserving its initial 0 state. As transistors MN2 and MN6 are still ON, node Q' is restored to its initial 0 state.

If the drain of transistor MP3 is hit by a particle, node M will go high, turning ON and OFF transistors MN1 and MP1 respectively. As transistors MN5 and MP5 are OFF, nodes Q and L become at high impedance conserving their states. As Q' is still low, transistor MP4 will remain ON restoring the state of node M that goes to 0.

Multiple SEUs can occur in the memory cell. HIT cells can manage with this problem. For example, if a particle strikes on M, this leads to turn OFF transistors MP1 and MP5, and if another particle strikes on Q, it turns transistors MN6 and MP6 OFF and ON respectively. Then node L is pulled down turning ON and OFF transistors MP2 and MN2 respectively and Q' goes high, turning ON and OFF transistors MN5 and MP5 respectively. Node M is asserted to 1 and node Q is asserted to 0. The contents of the memory cell are then corrupted. In a similar way it can be shown that simultaneous particle strikes on these nodes Q' and M lead to the corruption of the data stored in the memory cell.

Figure 6.10 presents the HIT2 memory cell. In the normal operation, if the RW signal is low (inactive) transistors MP1, MP4, MN2, MN5 and MN7 are ON the other transistors being OFF.

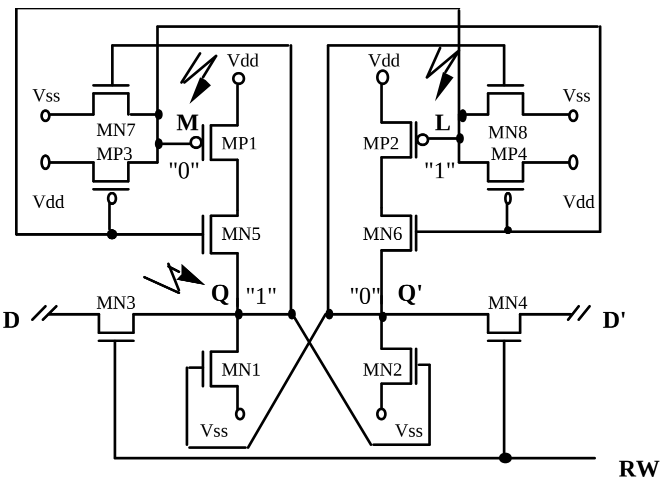


Figure 6.10 – The HIT2 memory cell

Then, it is easy to show that the logical states of nodes Q and Q' are conserved. Furthermore, as there are no direct paths from Vdd to Vss, the stability of HIT2 memorization function is guaranteed (the static current consumption is only due to the leakage current).

The reading of the HIT2 cell is performed by pre-charging to VDD data lines D and D'. As the read/write signal goes high, node Q will remain at 1 because MP1 and MN5 are both ON, while data line D', which is directly connected to node Q', will be discharged though transistors MN4, MN2.

To modify the state of the cell, the read/write signal should go high while the new values 0 and 1 are presented respectively at inputs D and D'. The 0 state of D will force at 0 node Q, turning OFF transistors MN2, MN7. Nodes M and Q' become at high impedance, node M conserve its state by capacitive effect, node Q' is pushed to 1 by data line D'. Transistors MN1, MN8 turn ON. Transistor MN1 confirms the 0 state of node Q. As transistors MP4 and MN8 are both ON, each of them attempt to impose a different state at node L, but an appropriate choice of the sizes of these devices ($W_{MN8} > W_{MP4}$) allows to push node L to 0 state through MP4. Transistors MP2, MP3 become ON, transistor MN2 turns OFF. Transistor MP3 push node M at 1, turning OFF transistors MP1 and MP4, and turning ON transistor MN6. Transistors MP2 and MN6 are then both ON, confirming node Q' to state 1. Line D imposes the '0' state to node Q, which is pushed to V_{dd} by two serial transistors MP1 and MN5. When Q goes to '0' state, transistor MN2 turns OFF allowing then node Q' to go to '1' state.

The HIT2 cell has also 3 sensitive nodes that are L, M and Q. HIT2 cell behaviors for each node SEU effect are described in next paragraph.

If a particle strikes the drain of transistor MN8, node L goes low and a transient '0' value appears at the gates of transistors MP2, MP3 and MN5. Transistors MP2 and MP3 are turned ON, transistor MN5 is turned OFF and node Q is not biased but conserves its '1' state by capacitive effect. Transistors MN7 and MP3 are both ON. They attempt to assign a different state to node M, but by design, the conductance of transistor MN7 is higher than the one of MP3 and then node M will conserve its '0' state. Because transistor MN6 is OFF, the ON state of transistor MP2 does not perturb node Q'. Transistor MP4 brings node L to its initial '1' state.

If a particle strikes the drain of the transistor MP3, node M goes high and a '1' appears at gates of transistors MP1, MP4 and MN6. Transistors MP1 and MP4 are then turned OFF, while transistor MN6 is turned ON. Nodes L and Q become floating but remain at '1' by capacitive effect. As transistor MP2 is OFF, the fact that MN6 is turned ON does not modify the state of node Q'. Node M goes to its initial '0' state through transistor MN7**.**

If node Q is upset by a particle, a '0' appears at the gates of transistors MN2 and MN7, that will turn OFF leading nodes Q' and M to a floating state. However, their initial '0' state is conserved by capacitive effect. Node Q is then restored to its initial '1' state.

HIT2 cell does not tolerate a double upset on Q, L or Q, M couples. This can be provoked either by the simultaneous strike of two particles or by a single particle with an appropriate incidence angle that crosses the two sensitive regions. Nevertheless, it is rather easy to show that HIT2 cell can recover errors provoked by double upset on L and M.

SEU testing presented in [VEL94] shows that the hardened HIT1 cell design is less sensitive at least by a factor of 10 than unhardened cell design. This immunity gain factor has been proved to be close to 5000 for particles having medium LET values (15 MeV*cm^2/mg). HIT cells can be used in CMOS devices providing 100% more area in each memory cell comparing to not hardened memory cells.

6.6 SGS Thomson memory cell

This cell has been proposed in [CAL96a], [CAL96b] and it has a logic level redundancy (LR cells) called DICE (Dual Interlocked CEll). This cell consists in a symmetric structure of four CMOS inverters, where each inverter has the n-channel transistor and the p-channel transistor separately controlled by two adjacent nodes storing the same logic state.

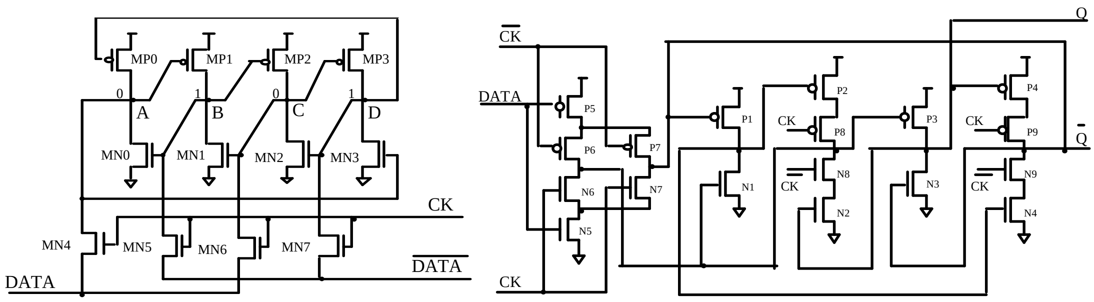
Figure 6.11 presents the DICE hardened memory cell and a latch built from DICE cell. The DICE memory cell has 12 transistors the same number of the HIT memory cells and IBM memory cell, but it has an advantage in terms of the transistor size.

The 4 nodes of the DICE cell form a pair of latches in two alternate ways, depending on the stored logic value. One of the adjacent nodes controls the conduction state of the transistor connecting the current node to a power supply line, and the other node blocks on the complementary transistor of the inverter, isolating it from the opposite supply line.

In Figure 6.11(a), the adjacent node pairs A-B and C-D have active cross-feedback connections and form two-transistor, state-dependent latch structures. The other adjacent node pairs, B-C and D-A, have inactive feedback connections (off transistors) which isolate the two latching pairs. Hence, two non-adjacent nodes are logically isolated and must be both reverted in order to upset the cell. If a charged particle hits a sensitive node, it flips the state logic and switches off the active feedback transistor controlling the adjacent latching node. The second node of the latching structure conserves its state by capacitive effect.

The inactive feedback transistor to the adjacent isolated node is switched on, and generates a logic conflict, which is propagated to the second latching node. The active feedback connections from the two unaffected nodes restore the initial state at the upset node and subsequently remove the state conflict of the second perturbed node.

A write operation in DICE cell is required to store the same logic state at two non-adjacent cell nodes in order to revert the logic state of the cell. Figure 6.11(a) presents the SRAM cell configuration with differential transmission gate R/W access. The DICE latch structure using clocked inverters is presented in Figure 6.11(b).



(a) (b)

Figure 6.11 – DICE hardened cell structure: a) latch b) flip-flop cell

Two circuit prototypes using the storage cell schematics of figure 6.11 in static RAM and register structures have been designed and processed using 1.2 µ CMOS/epi process from AMS [CAL96a], [CAL96b]. The first prototype is a 2K bit CMOS SRAM circuit composed of two sections using standard 6-transistor non-hardened SRAM cells and DICE hardened cells. The second prototype chip comprises three shift registers. One of the registers is built from standard, unhardened latches. The other two registers use two different DICE cell topologies, with and without transistor size and topology constraints, respectively.

The SEU immunity of the prototypes has been tested at the 68" cyclotron of Lawrence Berkeley Laboratories, Berkeley, CA. Under exposure at various particle energies it obtained a LET threshold for DICE cells around 50 $MeV/mg/cm^2$, compared to less than 10 $MeV/mg/cm^2$ for the unhardened cell [CAL96b].

6.7 Comparison between presented SEU Hardened Cells

Table 6.1 summarizes the main characteristics, advantages and drawbacks of the presented SEU tolerant memory cells. These SEU hardened memory cells are based on the main concept of memory value duplication into different parts of the cell making one of them able to restore the other using feedback paths.

Table 6.1 – Comparison between some SEU hardened CMOS memory cells

IBM memory cell		
Characteristics	Advantages	Drawbacks
• Memory cell has a total of 16 transistor with different size; • It is composed of 6 transistors to build the memory part, 6 p-channel transistors to SEU immune the latch and 4 transistor for read/write.	• technology process independent; • low static power dissipation; • good SEU immunity (LET up to 74 $MeV*cm^2/mg$).	• large number of transistors (16); • the size of transistors.
NASA Memory Cell I		
Characteristics	Advantages	Drawbacks
• This cell has 16 transistors with different size; • It is constructed of two parts, the top half part is composed of if only p-channel transistors and the other bottom half part has only n-channel transistors;	• technology process independent; • good SEU immunity (LET up to 120 $MeV*cm^2/mg$).	• large number of transistors (16); • the size of transistors. • static power dissipation
NASA Memory Cell II		
Characteristics	Advantages	Drawbacks
• This cell is an improvement of the Whitaker's SEU hardened CMOS memory cell. • This cell has 14 transistors.	• no static power dissipation. • reduced number of transistors (14).	• the size of transistors; • Above 30 $MeV.cm^2/mg$ the test chip latched up.
Canaris memory cell		
Characteristics	Advantages	Drawbacks
• It is composed of and-nors and or-	• SEU immune	• long recovery time

nands SEU immune cells.	technique for the combinational and sequential logic • good SEU immunity (LET up to 120 $MeV*cm^2/mg$).	after an upset; • leakage current problems that could appear due to total dose effects; • large number of transistors.
HIT1 and HIT2 memory cells		
Characteristics	Advantages	Drawbacks
• They are composed of 12 transistors organized as two storage structures interconnected by feedback paths.	• Small number of transistors; • less sensitive at least by a factor of 10 comparing to unhardened cell design (LET 52 $MeV*cm^2/mg$).	
SGS Thomson memory cell		
Characteristics	Advantages	Drawbacks
• It has logic level redundancy (LR cells) called DICE (Dual Interlocked CEll) • It is composed of 12 transistors. • It consists in a symmetric structure of four CMOS inverters.	• Small number of inverters; • Low power dissipation; • good SEU immunity (LET up to 50 $MeV*cm^2/mg$).	

Part II: SEU Mitigation Techniques for Programmable Logic Devices

7 Programmable Logic Devices

Programmable Logic Devices are widely used to implement logic circuits by offering the advantage of fast turnaround time, comparing to custom ASICs which present high recurring engineering cost and high risk, especially in limited production volume. However, ASICs still have a higher density, lower power and higher reliability than programmable circuits.

Programmable logic devices include Programmable Logic Arrays (PLA), Programmed Array Logic (PAL), Masked Programmable Gate Arrays (MPGAs) and Field Programmable Gate Arrays (FPGAs). PLA and PAL are defined as arrays of AND logic gates and OR logic gates. MPGAs are customized by the last metal layers. This customization is done in a technology process foundry. FPGAs are configured by the user and the customization is transferred into the chip by a computer cable.

Rapid prototyping is the key to quick turnaround in a product development process. Today's fast paced design cycles require the availability of early silicon and the flexibility of ramping to any volume production. Field Programmable Gate Arrays (FPGAs) are the most popular solution for the time-to-market because they can provide instant manufacturing and low cost prototyping. Since Xilinx Company [XIL98a] introduced the FPGA in 1985, many FPGAs have been developed by a number of other Companies like Actel [ACT98] and Altera [ALT98].

FPGAs continue to fall short masked gate arrays in performance, density and cost for high volume. Masked Programmable Gate Arrays (MPGAs), on the other hand, have longer turnaround times. New technologies and solutions have emerged to overcome the limitations of FPGAs while maintaining the benefits of traditional gate arrays [HOP99]. One solution is masked gate arrays customizable only by the topmost metal layer [DON93] called Quick Customizable Logic (QCL). Another solution for fast prototyping is the Laser Programmable Gate Array (LPGA).

Recently, Chip Express [CHI98] has introduced a new type of device between FPGAs and mask programmable gate arrays. This is based on laser cutting of metal interconnections in the laser programmable gate array (LPGA) or by a one-mask each. Both of these operations are done quickly at the company laboratories and do not require processing the die and wafers in a foundry.

LPGAs, MPGAs and FPGAs differ significantly in unit price, density, performance and prototyping lead times. Figure 7.1 shows different logic density and design time tradeoffs.

Figure 7.1 – Digital systems implementation options

A programmable logic circuit is based on logic blocks, interconnection blocks and IO blocks. All of them are programmable to implement the determined digital circuit.

The design flow of a programmable logic circuit synthesis is summarized in figure 7.2. Based in a high-level circuit description such as VHDL [SKA96], the circuit is described in the design flow. The project description is read and mapped into the specific logic blocks of the programmable matrix. The logic blocks are placed and connected in the matrix. The output of the design level is a file that contains all the matrix customization. This file can be load into the chip in the case of FPGAs and PLDs or can be used in the foundries to perform the mask customization of MPGAs.

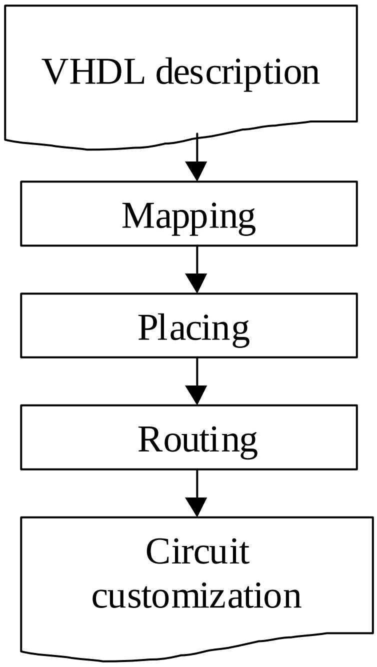


Figure 7.2 – Programmable logic device design flow

The use of programmable logic devices to implement reconfigurable logic and processors for spacecraft applications provides numerous benefits comparing to using ASICs devices. Design errors can be corrected after launch, higher performance can be achieved with software based processing, and using COTS devices can reduce costs. System performance can even be improved with updated hardware designs once on orbit performance is determined. ASICs have a disadvantage that their functionality may never be altered. As a result, not only it may never be updated, upgraded or corrected in any way, but any permanent destruction of its sub-circuits renders that portion of the circuit forever disabled. Both programmable and ASICs devices are composed of memory elements that can be affected by radiation.

The programmable logic devices are critically sensitive to SEU due to the large amount of memory elements located in these structures. Programmable logic devices must be strongly protected to avoid errors running in the space environment. There are two main ways to mitigate the radiation effects in Programmable Logic Devices:

- by VHDL description
- by matrix design implementation

7.1 High-Level Hardening Circuits

In the first solution, the VHDL can be modified in order to achieve reliability levels in the programmable devices. This technique consists in the substitution of the VHDL description of storage elements by hardened descriptions that can be implemented in the matrix. The modifications in the VHDL description can be done manually on the file description or automatically depending of the circuit architecture. No previous work was found about a automatically SEU mitigation technique in VHDL.

An example of mitigation technique in VHDL is based on EDAC [LIM00]. The Hamming Code protection and Reed-Solomon can be used to code and decode the values stored in the registers. In this way the value is corrected each cycle or each time that is read. For this technique it is possible to create an automatic tool to insert the codification and decodification logic blocks for all the registers.

Another method to mitigate the radiation effects automatically in the VHDL is using special library. This special library must be designed based on SEU hardened structures developed for programmable matrix. This solution has many advantages because this library can be developed to optimize performance, area and power dissipation according to the application and the programmable device family.

These techniques can be applied in all kind of logic circuits. However, they are not 100% efficient if they are performed in some kind of programmable matrix like FPGAs based in SRAM. All the customization elements (SRAM memory cells) inside the chip are vulnerable for radiation.

7.2 Hardening the Programmable Matrix

The second solution to SEU mitigation is based on the programmable matrix design. In this case, the programmable matrix is redesigned to be completely SEU hardened. This procedure is very expensive because it requires new projects and designs but it presents a high reliability. There is no available programmable matrix until now completely SEU hardened. One solution in this approach is to replace all the storage elements of the matrix by SEU Hardened memory, presented in section 6. No previous work was found about programmable matrix composed of SEU hardened memory cells.

The next sections present some mitigate solutions used nowadays by the programmable devices companies to reduce the programmable logic sensitive to radiation. The space and military market is still very new and a lot of thinks can be done to improve the programmable logic devices under radiation applications.

In section 8 some solutions in Masked Programmable Gate Arrays are presented. Some of these solutions change the architecture of standard MPGAs matrix. Section 9 presents SEU mitigate solution in FPGAs. These solutions do not change the FPGA matrix design but only the implementation approach. These solutions may differ from each other in terms of matrix area usage and performance.

8 Single Event Upsets Mitigation Techniques for MPGAs

Masked Programmable Gate Arrays are defined as matrix composed of programmable elements. These programmable elements can be pair of transistors or logic blocks located in rows. The matrix is customizable by the metal layers. To reduce the turnaround time and cost, some MPGAs are customizable only by the topmost metal layer. Figure 8.1 illustrates a typical MPGA matrix.

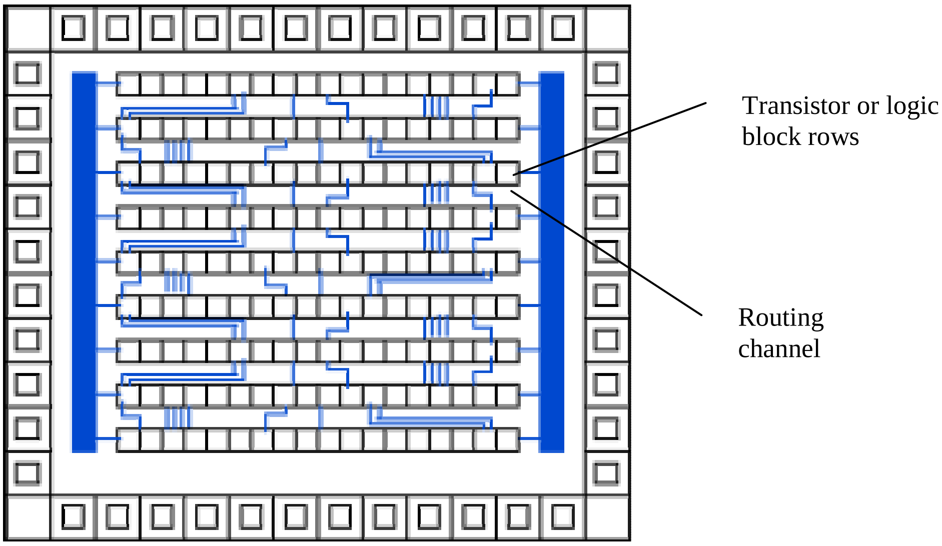


Figure 8.1 – MPGA matrix

One mitigation technique that can be applied in MPGAs is to use SEU hardened memory cell such as the cells presented in section 4. This technique changes the MPGA architecture and it is not a COTS solution.

Next sections show two different MPGAs developed in our university. Only the topmost metal layer customizes these approaches. One of them is named Ágata [CAR96] and it is composed of pair of transistors and the other is named Maragata [LIM99] and it is composed of logic blocks.

8.1 ÁGATA approach

Ágata is a masked programmable gate array composed of transistors designed like buffers that can be customized by the topmost metal layer [CAR96]. These transistors are located in rows separated by routing channels. The transistors NMOS and PMOS are connected during the matrix customization. And two beside transistors are isolated to each other by oxide. The NMOS transistors are connected to ground and the PMOS transistors are connected to the source.

Figure 8.2 shows its matrix architecture. The routing channel is predefined in metal 1 and the routing connection is done using the topmost metal layer.

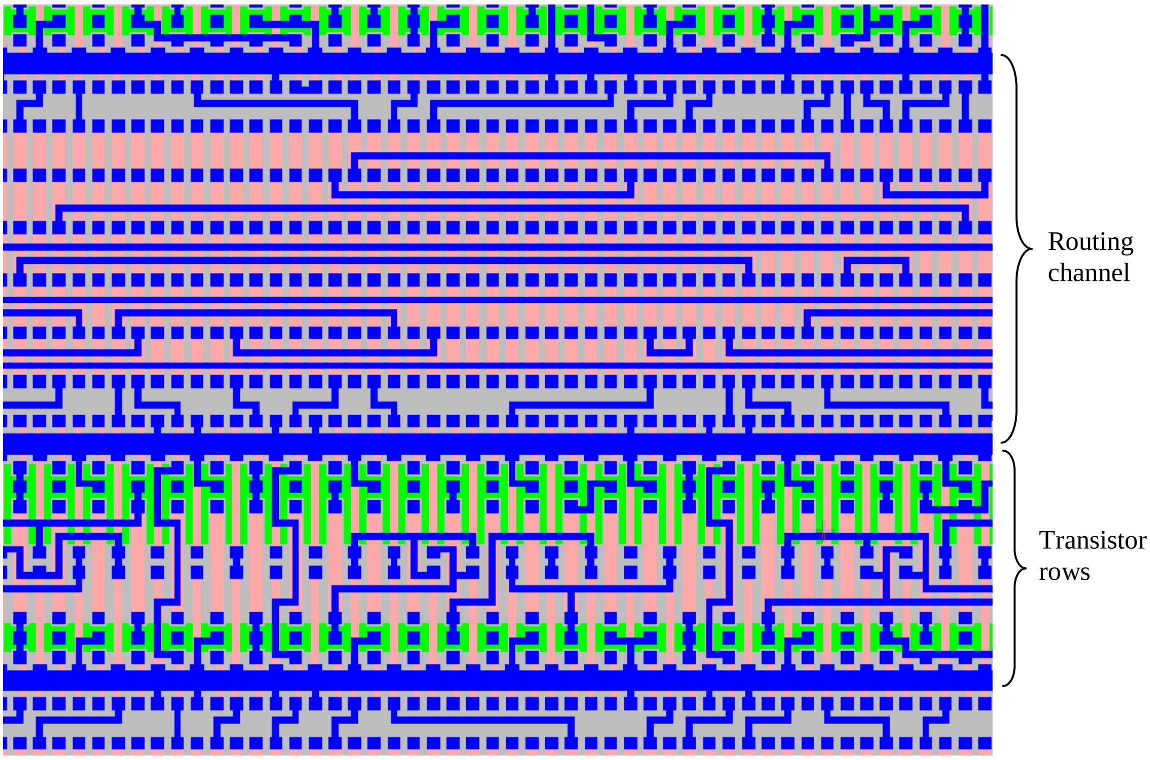


Figure 8.2 – Ágata matrix architecture

The Ágata transistors are designed as buffers because each transistor can be connected to any part of the matrix. Figure 8.3 exemplifies some pairs of transistors and their connections for the customization.

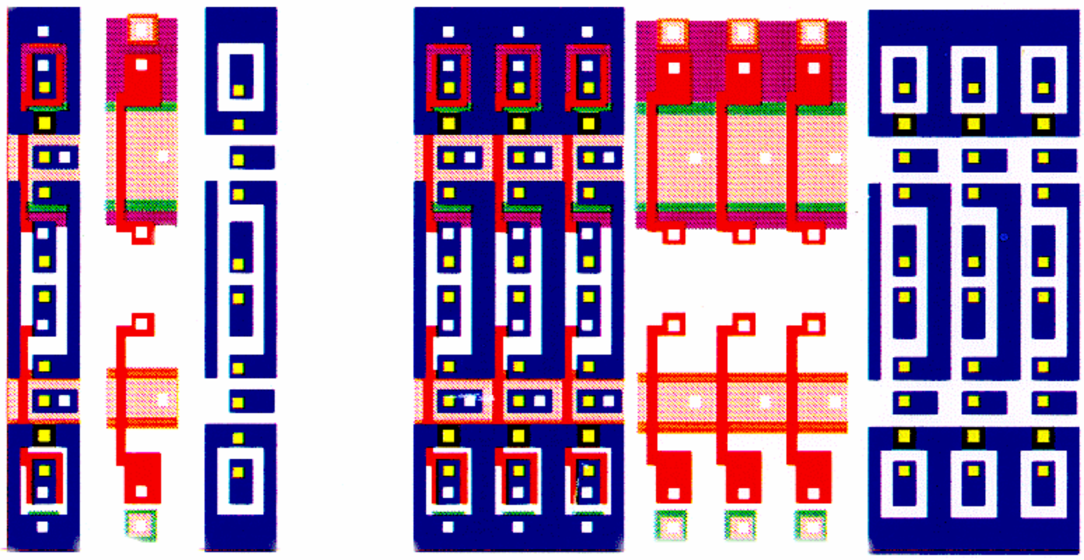


Figure 8.3 – Ágata matrix of transistors

The Ágata approach is based on library, in this way it is necessary to describe a circuit using the Ágata library cells to implement it in Ágata matrix. The library is defined as customization connections that must be done over the pair of transistors to implement such library cells (inverters, buffers, nands, nors, multiplexors, latches and flip-flops).

It is possible to improve this approach to use it in space applications building a new cell library using SEU hardened memory elements (figure 8.4). The standard latches and flip-flops can be replaced by hardened memory cell. The first step is to describe a hardened memory cell in terms of customization connections to implement it using the predefined pair of transistors.

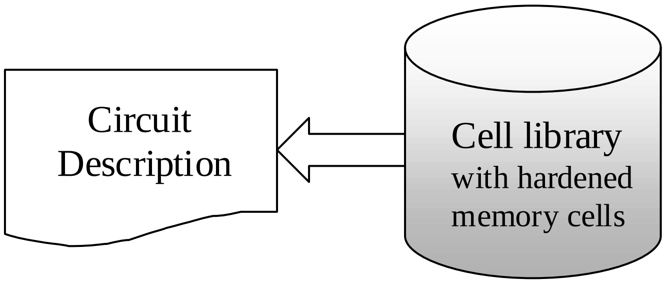


Figure 8.4 – Ágata cell library

This SEU mitigate technique has an advantage because it does not change the basic architecture of the matrix, only the software implementation must be updated.

8.2 Maragata Approach

Aiming at increasing logic density of digital implemented in programmable matrixes, a new methodology based on mask programmable matrix customizable by the top most metal layer was proposed in [LIM98]. In this new approach called Maragata, the transistor rows are replaced by programmable logic blocks that can be specifically named as Universal Logic Gates (ULGs). Maragata is composed of coarse grain ULGs like in a hard-wired version of a FPGA architecture that combines the efficiency of MPGAs with the flexibility of FPGA architecture. Its ULGs were developed considering the implementation of sequential and processor-like circuits, because these ULGs can implement latches or flip-flops with low area cost.

The large flexibility of ULGs justifies its use for building up programmable matrix, particularly when customization is performed by using the topmost metal layer. When a more complex cell is used for building MPGAs, it is possible to optimize silicon area by properly sizing its transistors. Moreover, in such approach the transistor connections as well as small connections are already done. For instance, internal cell transistors that do not have to drive large capacitive loads may be smaller or even of minimum size. Overall timing performance of the cell is assured by sizing output cells as buffers by the time the matrix is designed.

The proposed ULGs to Maragata can implement either combinational logic or sequential logic. Figure 8.5 presents the ULGs designed to Maragata approach. Most of FPGAs have logic blocks that can implement combinational logic. To implement sequential logic it is necessary a flip-flop per logic block. When this logic block is used only for combinational logic, the flip-flop area is wasted. The ULG3 can implement a flip-flop master-slave (with set and reset) using its multiplexors. It is necessary two

ULG3 to implement one flip-flop and only one CLUS2 to implement the same flip-flop. It has been done some research to select a good ULG among these ones, looking for low granularity, high flexibility and the availability of a technology mapper [LIM99].

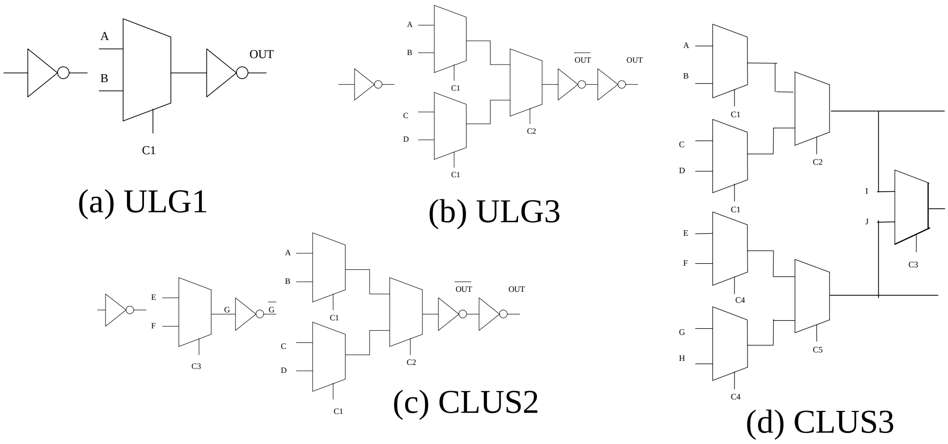


Figure 8.5 - ULGs developed to Maragata

Multiplexors were implemented by using transmission-gates rather than by CMOS static gates, to minimize not only transistor count, but power dissipation as well. In this ULG there are at most two transmission gates in series in a path between two buffers, ensuring good signal propagation. In order to achieve minimal layout area, minimum width transistors were used whenever it is possible. In each ULG output transistors were sized to work as buffers. These transistors have the same size of Ágata transistors [CAR96] and offer the same fan-out, but the buffers can be bigger. The number of customizable points is the most severe constraint in ULG layouts. Internal fixed and customizable cell connections may contribute to reduce channel routing complexity.

Figure 8.6 presents a circuit layout implemented in the Maragata matrix. The customization is done in metal 2. This matrix is composed of 26 rows, 80 pads and has 1040 ULG3s. The matrix area is about 11.03 mm^2. Its logic density is 2263 tr/mm^2. It is important to notice that the routing channel takes a significant area. By reducing connections one can expect a large reduction in the total matrix area.

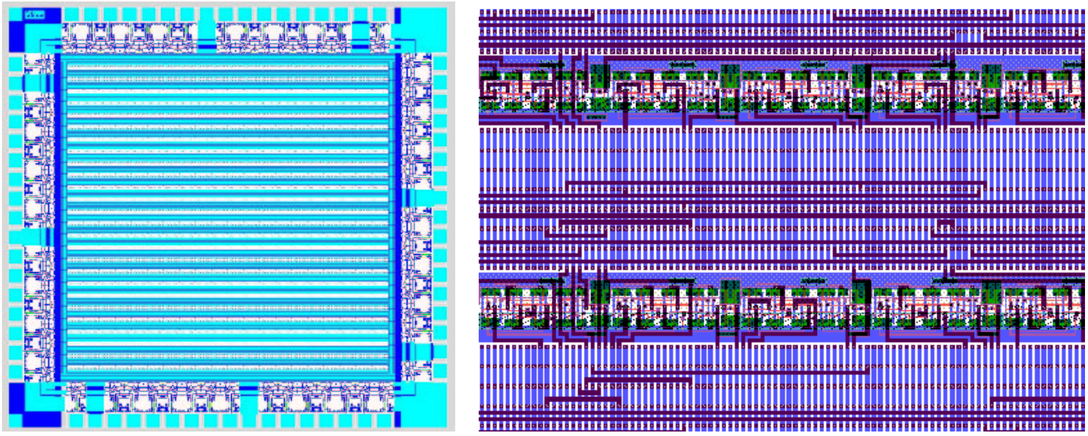


Figure 8.6 – Matrix layout (the routing channel, the ULG rows and the customization in metal 2).

Figure 8.7 shows the layout of two ULGs in a standard 0.8 μm double metal CMOS technology, with Metal 2 grid running on vertical lines.

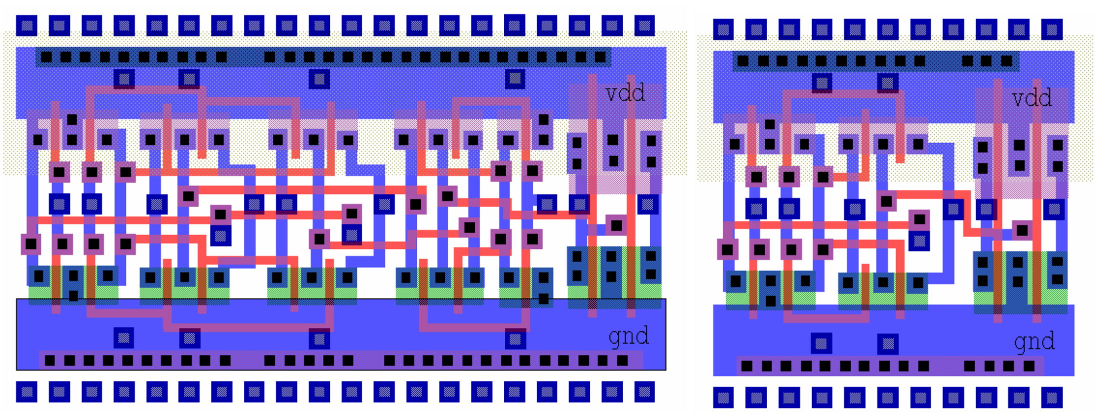


Figure 8.7 – ULG3 and ULG1 layouts in a double metal process

Table 8.1 shows the number of transistors and area for all developed ULGs. All the customizable connections are done over the ULG without using the routing channel. The first metal layer was used for internal connections, while the second one was reserved for customization. Table 8.1 also presents the area comparison for a master-slave flip-flop implemented into different ULGs. The cell CLUS3 can either implement 1 bit register or a D flip-flop. The area of a flip-flop using Ágata implementation is 5528 μm^2.

Table 8.1 – ULGs Characteristics

ULG	# transistors	Area (μm^2)	# ULGs to implement a flip-flop	Area (μm^2) of a flip-flop
ULG1	10	1057	4	4228
ULG3	22	1922	2	3844
CLUS2	30	3000	1	3000
CLUS3	50	5000	1	5000

Mapping some medium combinational and sequential circuits provides comparisons in terms of area gain. For these circuits, the use of ULGs resulted in area gains around 20% for almost all examples. It was also calculated the number of required connections for different examples, showing that the Maragata approach leads to effective reduction in the number of connections. These gains can represent a logic density improve because more connections can be done in the same routing channel. Figure 8.8 shows two examples of a circuit implemented in Maragata and Ágata approach.

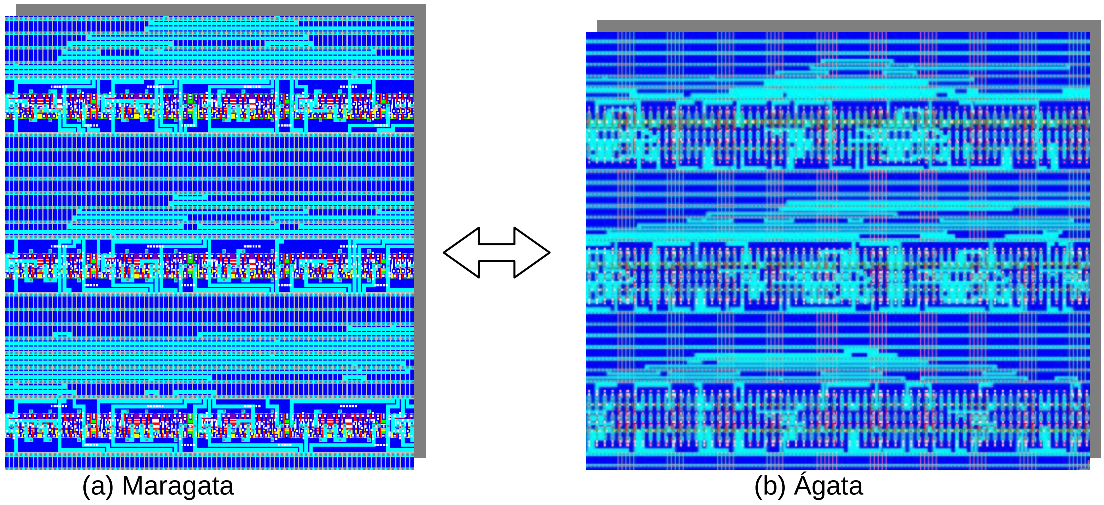


Figure 8.8 – Maragata and Ágata matrix implementing a digital circuit

Maragata approach has the peculiarity of using combinational logic to implement flip-flops and latches as shown in figure 8.9. Analyzing the schematic presented in figure 8.9, we can see that a charged particle hit in a transistor may not cause a bit-flip in the flip-flop because of the structure of the multiplexor that are composed of transmission gates and of the output inverters delay. For this reason, by its construction the Maragata matrix is low SEU sensitive. However, due to the decreasing of transistor features such as gate dimensions and power supplies, the combinational part can be also affected by charged particles in space applications.

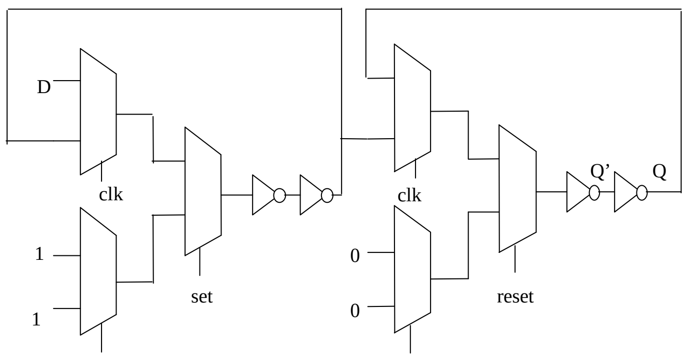


Figure 8.9 – Maragata logic cell implementing a flip-flop

Moreover, it is possible to change the Maragata matrix topology to turn it effective SEU hardened by using hardened memory cells. The ULG3 for example can be replaced by another logic block composed of two parts: the combinational part and a SEU hardened flip-flop as it is showed in figure 8.10. In this way, the ULG continues to implement the same number of functions but the same ULG can implement a sequential part that it is SEU immune.

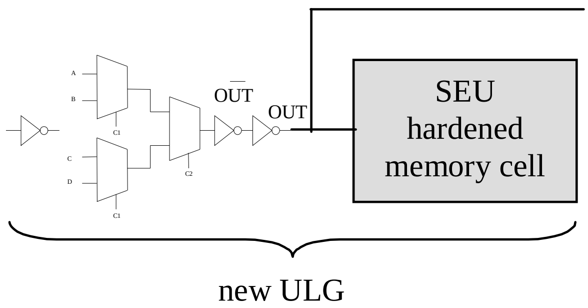


Figure 8.10 – Maragata SEU hardened ULG

This mitigate technique has the disadvantage of changing the matrix topology but it can solve efficiently the SEU problem.

<u>*MPGA Resume*</u>*: In MPGAs, the storage elements can be implemented in the matrix by organizing the combinational logic blocks in order to build memory cells or by using specific memory cells that are already placed in the matrix or described in a customization library. The SEU mitigation technique can be done by describing SEU hardened memory cells in the customization library or by designing the SEU hardened memory cells in the matrix. The first solution can be easily applied in a gate array matrix composed of pair of transistors. The second solution may be implemented in a matrix composed of more complex logic blocks as presented in this section.*

9 Single Event Upsets Mitigation Techniques for FPGAs

Field Programmable Gate Arrays are becoming increasingly popular with spacecraft electronic designers as they fill a critical niche between discrete logic devices and the mask programmed gate arrays. The devices are inherently flexible to meet multiple requirements and offers significant cost and schedule advantages. Because of FPGAs are re-programmable, data can be sent after launch to correct errors or improve the performance of spacecraft.

The architecture of a programmable device is based on an array of logic blocks that can be programmable by the interconnections to implement different designs. A FPGA logic block can be simple as small logic gate or as complex as clusters composed of many gates. Current commercial FPGA's logic blocks are composed of one or more of transistor pairs, basic small gates, multiplexors, Lookup tables, and-or structures.

The routing architecture incorporates wire segments of various lengths, which can be interconnected via electrically programmable switches. The distribution of the different length wire segments affects the density and the performance of the FPGA. For example, if many short wire segments are used, the long interconnections are implemented using many programmable switches and the result is large delays. Using an inadequate number of segments, some parts of the logic block may not be used, the result is a low logic density.

Several different programming technologies are used to implement the programmable switches. There are three types of such programmable switch technologies currently in use:

- *SRAM*, where the programmable switch is a pass transistor controlled by the state of a SRAM bit (SRAM based FPGAs)
- *Anti-fuse*, when an electrically programmable switch forms a low resistance path between two metal layers. (Anti-fuses based FPGAs)
- *EPROM, EEPROM or FLASH cell*, where the switch is a floating gate transistor that can be turned off by injecting charge onto the floating gate. These programmable logic circuits are called EPLDs or EEPLDs.

Both customizations based on SRAM and anti-fuses are volatile. The EPROM and EEPROM customization are non-volatile. Each of them has particular architecture and logic blocks in its matrix. Table 9.1 presents the main programmable elements.

Table 9.1 – Customization technology characteristics

Technology	volatile	Re-programmed	Chip area	R(ohms)	C(fF)
SRAM	Yes	In the circuit	Large	1-2K	10-20
Anti-fusível (Plice)	No	No	Small	300-500	3-5
EPROM	No	Out of the circuit	Small	2- 4K	10-20
EEPROM	No	In the circuit	2xEPROM	2- 4K	10-20

Table 9.2 shows characteristics of some commercial FPGAs.

Table 9.2 – Commercial FPGAs and PLDs characteristics

Company	Architecture	Logic Block	Technology	Example of families
Xilinx	Symmetric Array	Look-up Table	SRAM	XC4000, Spartan, Virtex
Xilinx	Hierarchy Array	OR-AND array	FLASH	XC9500
Actel	Row based Array	Multiplexors	Anti-fuse	SX, MX
Altera	Symmetric Array	Look-up Table	SRAM	Flex8K, Flex10K, FLEX20K
Altera	Hierarchy PLD	OR-AND array	EEPROM	MAX7000, MAX8000, MAX9000

Figure 9.1 shows a portion of a FPGA matrix with the logic blocks (CLBs), the interconnection programmable switch matrix (PSM) and different length wire segments.

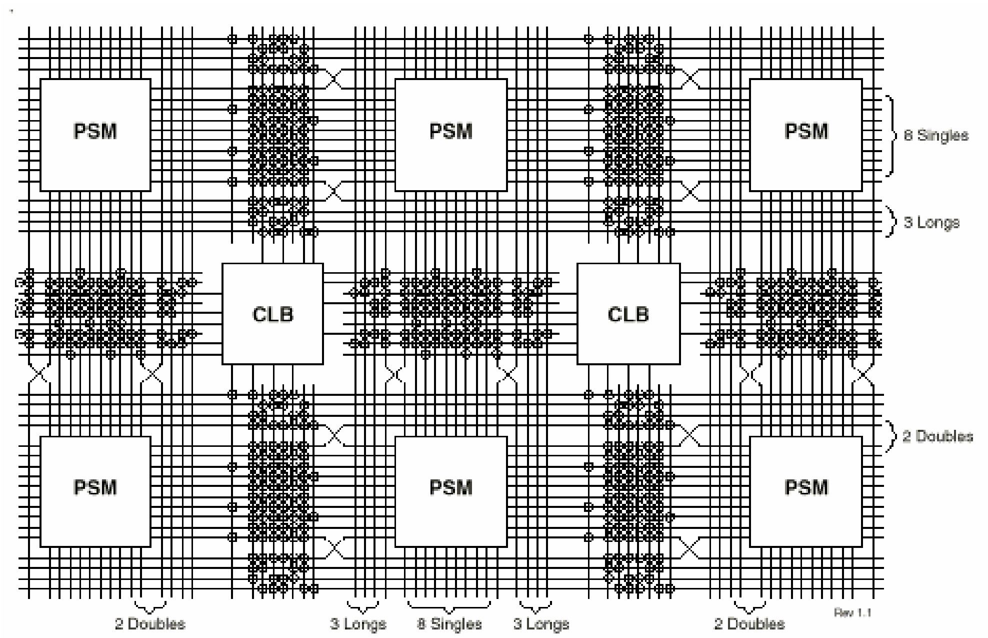


Figure 9.1 – Detail of the FPGA matrix from Xilinx XC4000 family

Architecturally, the choice of the type of storage for the configuration information in the FPGA and the type of the logic block drives the radiation sensitivity in the device. Each kind of FPGA, based on SRAM, Anti-fuses or EEPROM/FLASH, has different levels of SEU sensitivity and peculiar SEU mitigate techniques. Additionally, the choice of fabrication technology affects the TID and single event latchup protection while determining die size, operating speeds, and power dissipation. The diversity of FPGA technologies and architectures do evaluating the radiation effects complex at both the device and system level.

Next sections aim to describing SEU mitigation techniques for the most popular commercial FPGAs.

9.1 SEU Mitigation Techniques for SRAM based FPGAs

SRAM based FPGAs are fast programmed by loading a configuration bitstream (collection of configuration bits) into the device. The device functionality can be changed at anytime by loading in a new bitstream. For this reason a very important application of SRAM based FPGAs is reconfigurable architectures. For this reason they are the most appropriated FPGAs for space applications (for example satellites, spacecraft, airplanes, etc…) where the reconfigurable capability can be very interesting to solve problems and to increase performance.

However, SRAM based FPGAs are strongly susceptible to radiation upsets because in these devices a high number of latches define all the logic functions and the on-chip interconnects. The upsets in these latches can cause circuit operation changes, and not just cause a burst of invalid data. Such latches are similar to the 6-transistor storage cells used in SRAMs, which has proved to be sensitive to single event upsets caused by charged particles. To solve this drawback, SEU mitigation techniques are required.

The company that succeed the market of SRAM based FPGAs nowadays is Xilinx. One of the most fast and density families of FPGA developed by this company is the Virtex family [CAM99]. Virtex has become a common ASIC replacement in commercial markets due to its density, performance, and wide range of capabilities. Its structure is composed of an array of complex logic blocks (CLBs) based on LUTs and routing connections programmed also by SRAM cells.

Altera is another prosperous company that fabricates SRAM-based FPGAs. The families are called FLEX. They present many types of FPGAs with different densities and performance. However, Altera does not have proposed until now a Hardened FPGA family. Because of this fact, this report will address only the SRAM FPGAs fabricated by Xilinx.

Let’s first analyze the topology of the SRAM FPGAs in more details. Figure 9.2 starts presenting the topology of the Virtex family. It is composed of array of complex logic blocks, programmable matrixes and routing segments. This family has also embedded memories that can work as memory or complex logic functions. Virtex family can be partial reconfigured, which can make a great advantage in many applications.

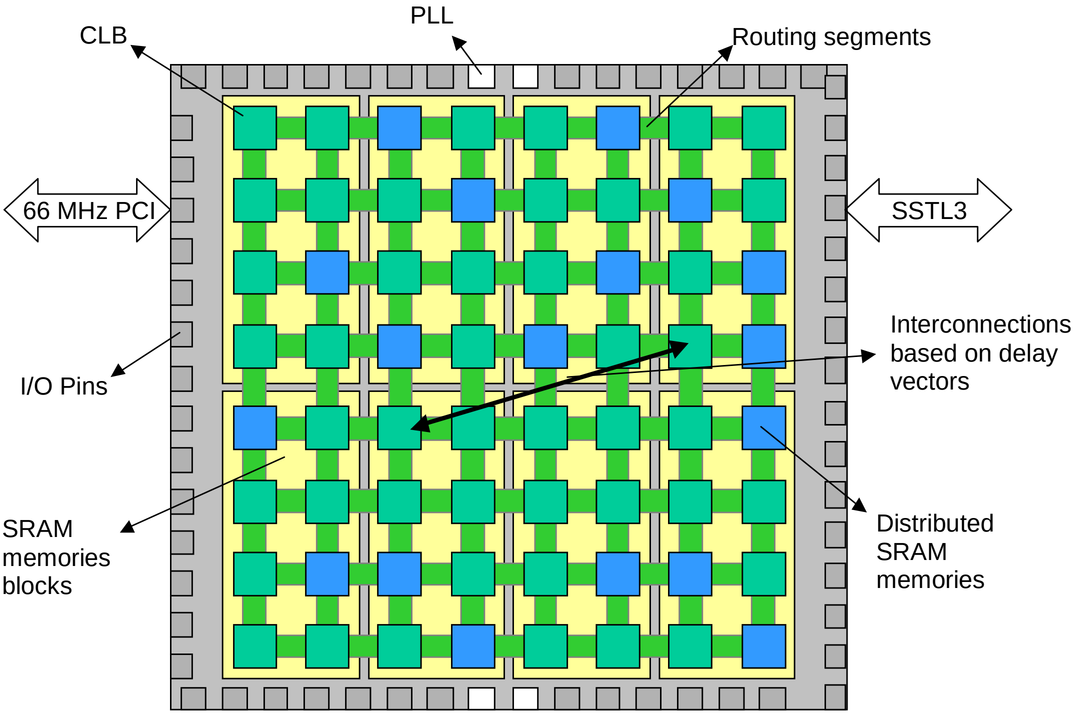


Figure 9.2 – SRAM based FPGA topology

The CLB of Vitex family, figure 9.3, is composed of 3 LUTs connected by multiplexors. A LUT is a block of memory and it implements any function up to *n* inputs, where *n* is a fixed number greater than 2.

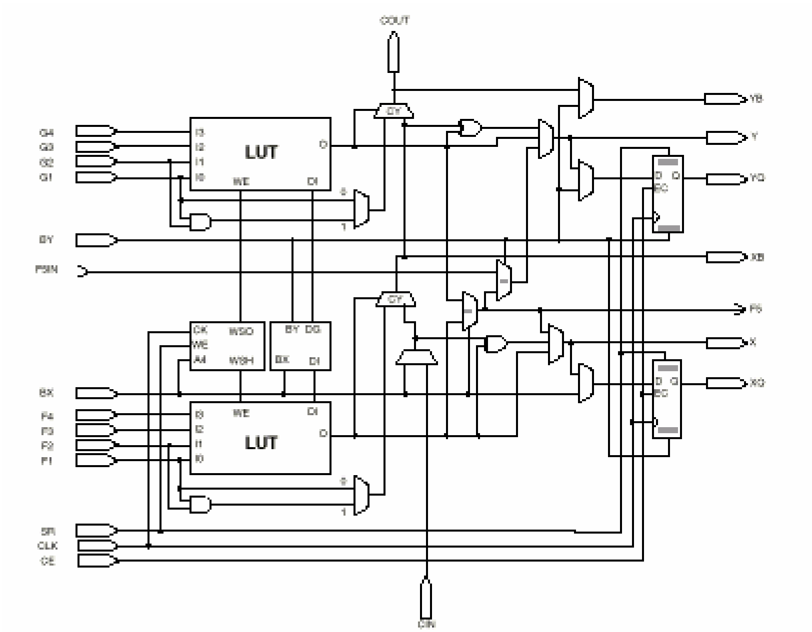


Figure 9.3 – Virtex family CLB

The SRAM cells connected to the block inputs do the customization of the CLB. The interconnections are programmed by the switch elements that are controlled by SRAM cells too. Figure 9.4 illustrates the programmable switch matrix (PSM). Each gate of the pass transistor is connected to a SRAM cell.

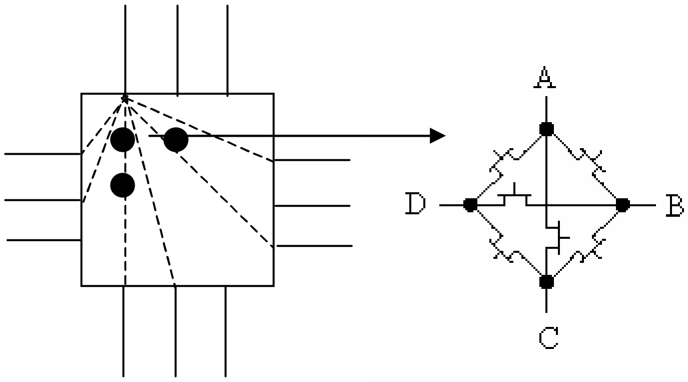


Figure 9.4 – Detail of the customization element in the matrix

Another example of CLB is shown in figure 9.5. This logic block is from the XC4000 and Spartan family. The difference between these two families is the amount of memory inside. The Spartan has embedded memories like the Virtex.

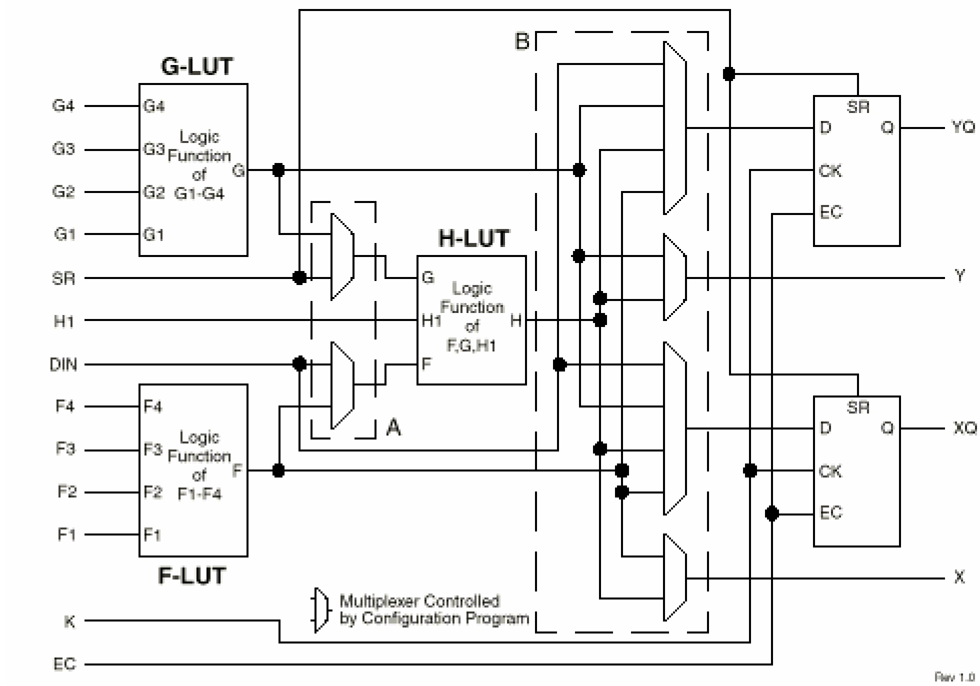


Figure 9.5 –XC4000 and Spartan family CLB

A resume of the Xilinx radiation hardened products is presented in table 9.3.

Table 9.3 – Radiation hardened products

Family	*Devices*	*Features*
XC/XQ4000/E/EX	XC4005/E, XC4010/E, XC4013/E, XC4025E, XQ4028EX	• 5000-28,000 gates • Up to 256 user I/Os • Extensive system features includes on-chip user RAM
XQ4000XL	XQ4013XL, XQ4036XL, XQ4062XL, XQ4085XL	• Up to 180,000 system gates • 3.3V, 5V compatible I/O
XQR4000XL	XQR4013XL,	• Up to 130,000 system gates

Radiation Hardened	XQR4036XL, XQR4062XL	• 60Krads total dose, latchup immune
Virtex	XQV100, XQV300, XQV600, XQV1000	• Up to 1,000,000 system gates • 2.5V
Virtex Radiation Hardened	XQVR300, XQVR600, XQVR1000	• 100K-rads total dose, latchup immune

The Xilinx XQVR product line is a radiation-tolerant version of the commercial Virtex series and XC4000 series FPGA. The XQVR utilizes a 7-micron epitaxial[1] layer process that renders it latch-up immune to a LET of 125MeV-cm^2/mg.

The main problem of using SRAM based FPGAs for space applications is that all the circuit are SEU sensitive because either the combinational parts, the sequential parts and the routing customization are implemented in the matrix using latches that are SEU sensitive.

There are three types of memories to be protected against SEU in a SRAM based FPGA. The first are the memory cells that compose the LUTs and the flip-flops of the CLB located in the "first floor" of the configuration hierarchy. The second are the memory cells that program the logic blocks (CLBs) located in the "basement". And final are the memory cells that program the interconnections, located also in the "basement". See the configuration hierarchy in figure 9.6.

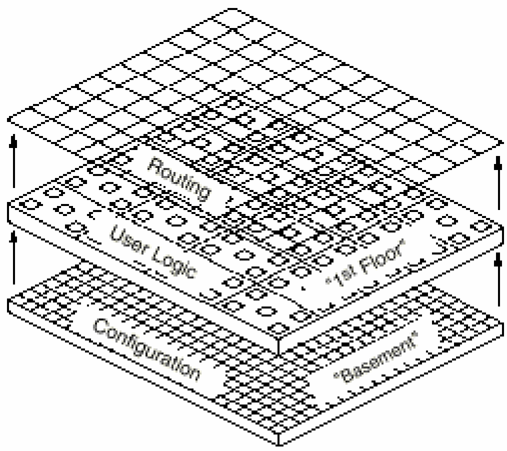


Figure 9.6 – Xilinx FPGAs configuration hierarchy

Next paragraphs discuss some solutions to mitigate single event upsets in SRAM based FPGAs [KAT94], [KAT97], [XIL98b] and [CAM99].

9.1.1 Module Redundancy

A very simple method for implementing SEU mitigation in a users' FPGA design is to replicate redundant instances of an entire module and mitigate the error effects at the final outputs of the modules using a voter. The clear advantages of this example of module redundancy is that it may be a single chip solution (an important

[1] http://my.netian.com/~jinimp/semi/_epitaxy.html)

cost advantage) and will not impact system performance. The obvious disadvantage is the limitation on the design size (less than 1/3 of the total device).

However, most SRAM based logic devices cannot reliably implement the voter function because the voting circuit itself would have to be implemented in SRAM cells just as any other Boolean function would be, and is therefore itself equally sensitive to upsets. The Virtex architecture provides a solution to implementing this circuit reliability by using the Tri-State Buffers (BUFTs) that are composed of a hard-wired AND-OR logic structure [ALF98].

In this case the tri-state buffers implement the voter as it is shown in figure 9.7.

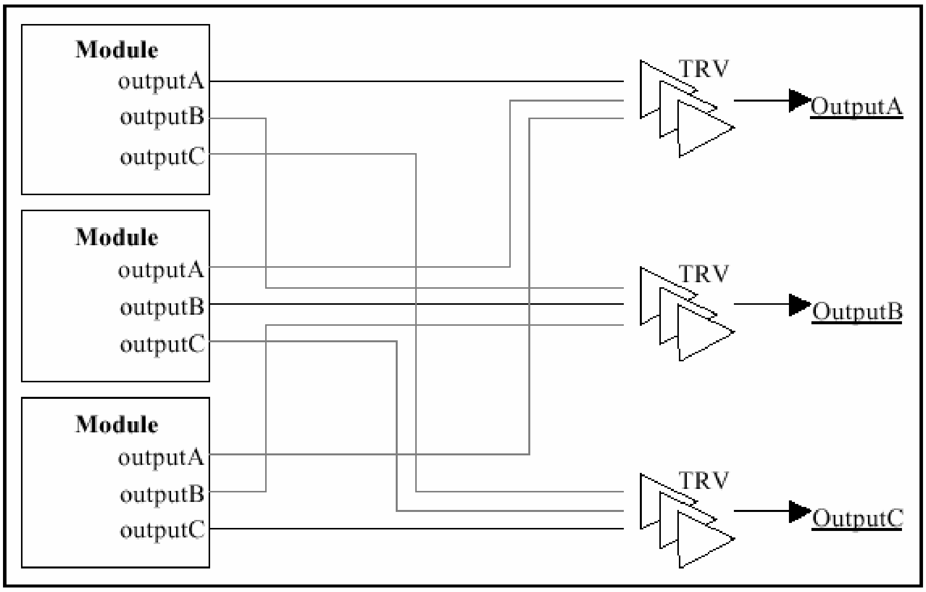


Figure 9.7 – Module redundancy

- ***Logic Partitioning and Redundancy***

In the case where the total design is more than 1/3 of the device size, the design could be partitioned into modules small enough to be replicated and mitigated within a single device, and spread across several devices. Such a solution is presented in Figure 9.8. This partitioning can reduce the performance of the project because the interconnections are done outside the FPGA and represent an added cost not only for the multiple FPGAs, but for the increased board space utilization as well.

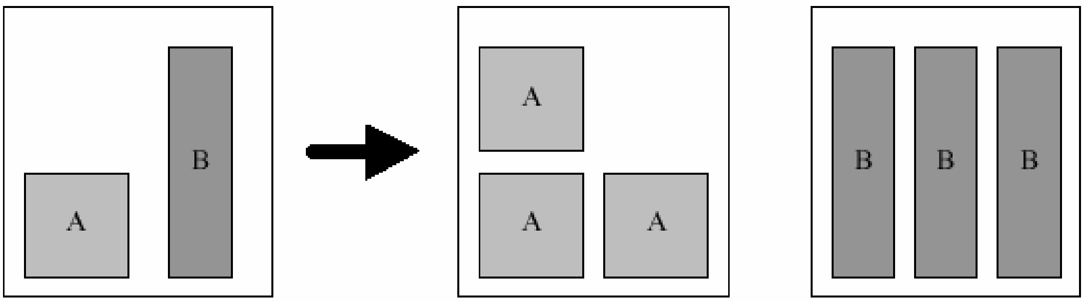


Figure 9.8 – Module partitioning

- ***Logic Duplication***

In the case where the design is less than ½ the size of the total device, an alternative to logic partitioning is logic duplication. If logic is duplicated and the outputs compared, whenever one set of outputs differs an SEU has been detected. This method is presented in figure 9.9 when the modules A and A' are duplicated in two FPGAs. The disadvantages of this method is the use of multiple FPGAs however it does not represent a decrease in performance because all the project is in the same FPGA and it does not need a external circuit for mitigation. In case of a total device failure, the other device can continue working. Important, this approach is only suitable for SEU detection. It is not enough for SEU correction.

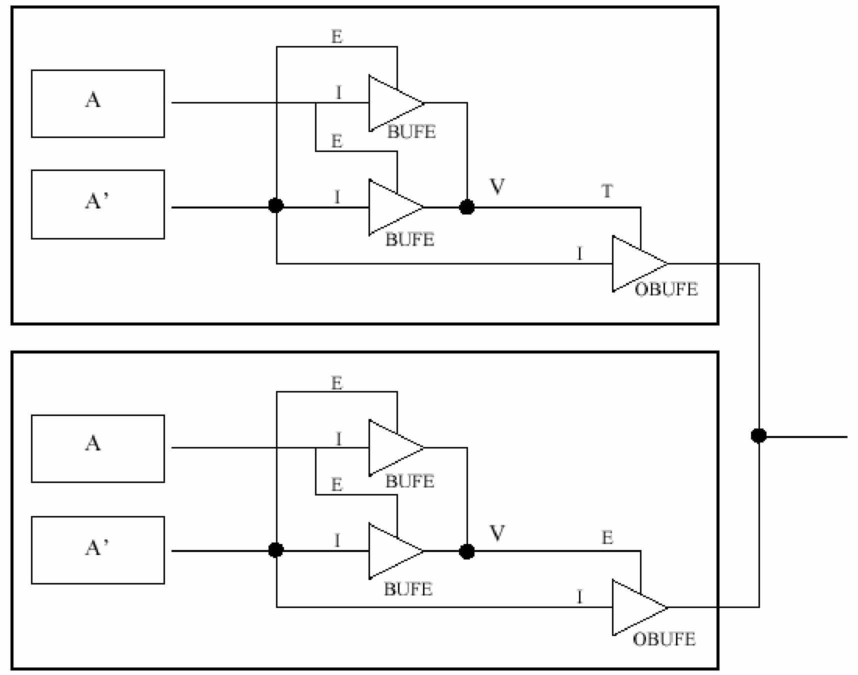


Figure 9.9 – Dual voting double redundancy

9.1.2 Device Redundancy

A commonly known method for SEU mitigation is "triple module redundancy with voting." This mitigation scheme uses three identical logic circuits performing the same task in tandem with corresponding outputs compared through a majority vote circuit.

Triple device redundancy and mitigation is until now the most rock-solid mitigation method for SRAM based FPGAs. This is shown in Figure 9.10. It has the highest reliability for filtering single and multiple events upset, transients upsets, and any other functional interrupts including total device failure. However, this is also a more costly solution comparing to the triple modular redundancy and it is not able to correct upsets either.

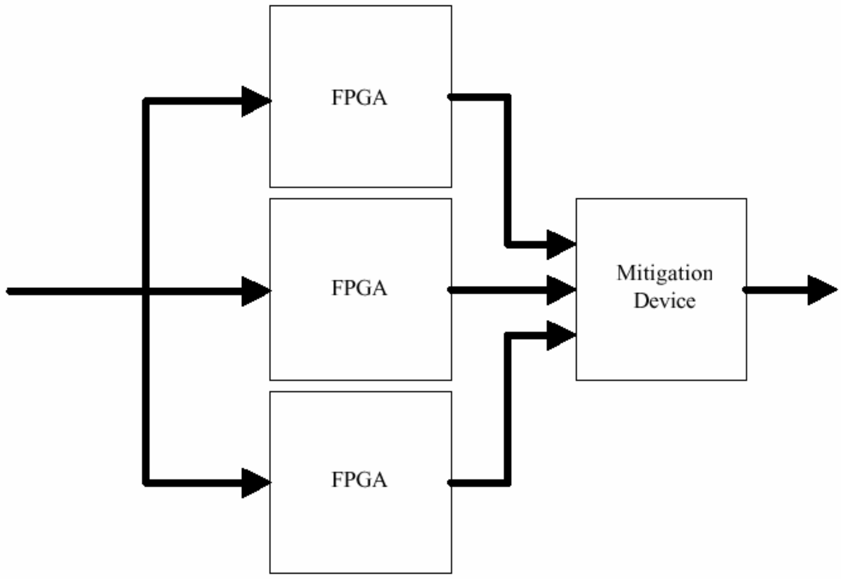


Figure 9.10 – Triple device redundancy

Figure 9.11 illustrates an implementation of a double modular redundancy in a XC4000 FPGA under a double device redundancy. This is a double way to protect the circuit. However, it has the same limitations mentioned before.

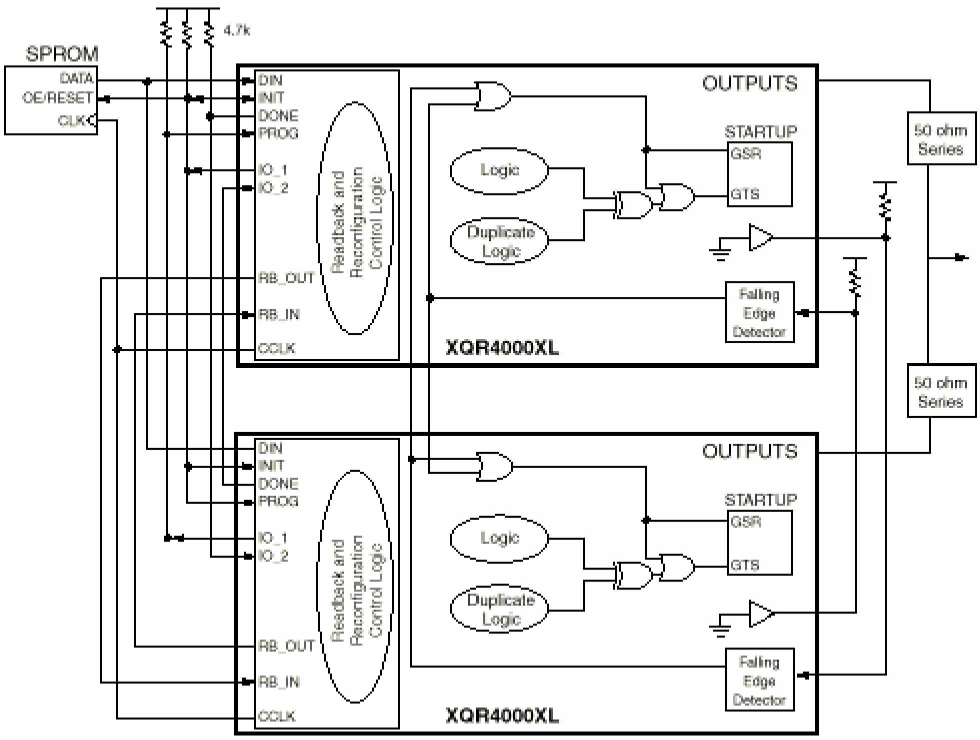


Figure 9.11 – Double device redundancy with voter

9.1.3 Correcting SEU through Partial Configuration

A good SEU mitigation technique should filter out the effects of upsets, during their short existence, as well as filter out the results of transient upsets. In some systems

SEU detection and correction errors by partial configuration can achieve an acceptable level of reliability. However, for applications where an even higher level of reliability is needed, or simply that any interrupt in service is unacceptable, other SEU mitigation techniques may be applied.

This section presents some mitigation techniques using the bitstream of the Virtex series. Aiming to understanding better the configuration mode, some capabilities of the Virtex reconfiguration array are presented first.

The Virtex family from Xilinx has an architecture that supports partial reconfiguration mode, which gives numerous advantages [XIL00b]. Each Virtex device contains, figure 9.11:

- configurable logic blocks (CLBs) that provide the functional elements for constructing logic
- IOBs that provide the interface between the package pins and the CLBs
- Dedicated Block SelectRAM (BRAM) of 4096 bits each (figure 9.12).
- Clock DLLs for clock-distribution delay compensation and clock domain control.
- 3-State buffers (BUFTs) associated with each CLB that drive dedicated segmented horizontal routing resources.

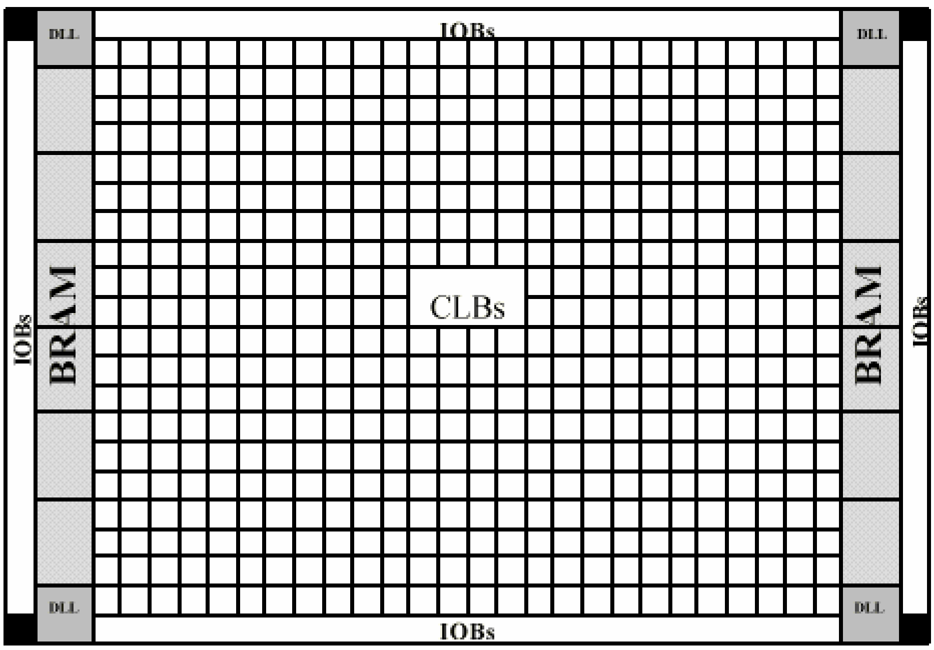


Figure 9.11 – Virtex architecture overview

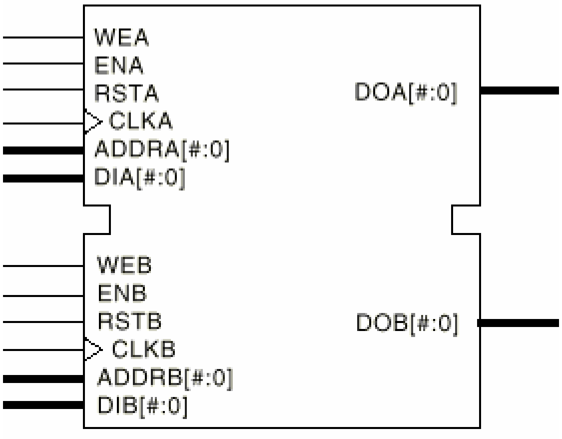


Figure 9.12 – Dual-port SelectRAM block

Configuration bitstream can be read and written through one of the configuration interfaces of the device named the *Virtex Series FPGA SelectMAP* (Selectable Microprocessor Access Port) interface. SelectMAP is an 8-bit parallel bi-directional synchronous interface to the configuration control logic designs. This interface provides post-configuration read/write access to the configuration memory array. "Readback" is a post-configuration read operation of the configuration memory, and "Partial Reconfiguration" is a post-configuration write operation to the configuration memory. Readback and Partial Reconfiguration allow a system to detect and repair SEUs in the configuration memory without disrupting its operations or completely reconfiguring the FPGA.

The bitstream is a series of configuration commands and configuration data, as shown in figure 9.12, where CMD means configuration command and DATA is the configuration data.

CMD1	data	CMD2	data	CMD3	data	CMD1

Figure 9.12 – Bitstream example

The Virtex configuration memory can be visualized as a rectangular array of bits. The bits are grouped in vertical frames that are one bit wide and extended from the top of the array to the bottom. Frames are grouped to compose different columns. A frame is the smallest portion of the configuration memory that can be written to or read from. Table 9.4 presents all the categories columns.

Table 9.4 – Virtex Configuration Column Type

Column Type	# of frames	# per device
center	8	1
CLB	48	# CLB columns
IOB	54	2
Block SelectRAM interconnect	27	# of blocks SelectRAM columns
Block SelectRAM content	64	# of blocks SelectRAM columns

The configuration memory array is divided into three separate segments:

- CLB Frames,
- BRAM0 Frames
- BRAM1 Frames

The two *BRAM segments* contain only the RAM content cells for the Block SelectRAM elements (column: Block SelectRAM content). The BRAM segments are addressed separately from the *CLB Array*. Therefore, accessing the Block SelectRAM content data requires a separate read or write operation. Read/Write operations to the BRAM segments should be avoided during post-configuration operations, as this may disrupt user operation.

The *CLB Frames* contain all configuration data for all programmable elements within the FPGA (all other columns). This includes all Lookup Table (LUT) values, CLB, IOB, and BRAM control elements, and all interconnect control. Therefore, every programmable element within the FPGA can be addressed with a single read or write operation. All of these configuration latches can be accessed without any disruption to the functioning user design, as long as LUTs are not used as distributed SelectRAM (BRAM) components.

While CLB flip-flops do have programmable features that are selected by configuration latches, the flip-flop registers themselves are separate from configuration latches and cannot be accessed through configuration. Therefore, readback and partial configuration will not effect the data stored in these registers.

However, when a LUT is used as either a distributed SelectRAM element (BRAM), or as a shift register function, the 16 configuration latches that normally only contain the static LUT values are now dynamic design elements in the user design. Therefore, the use of partial reconfiguration on a design that contains either LUT-RAM (i.e., RAM16X1S) or LUT-Shift-register (SRL16) components may have a disruptive effect on the user operation. For this reason the use of these components can not be supported for this type of operation.

However, Block SelectRAMs (BRAM) may be used in such an application. Since all of the programmable control elements for the Block SelectRAM are contained within the CLB Frames and the BRAM content is in separate frame segments, partial reconfiguration may be used without disrupting user operation of the BRAM as design elements.

Figure 9.13 shows columns of a sample Virtex device.

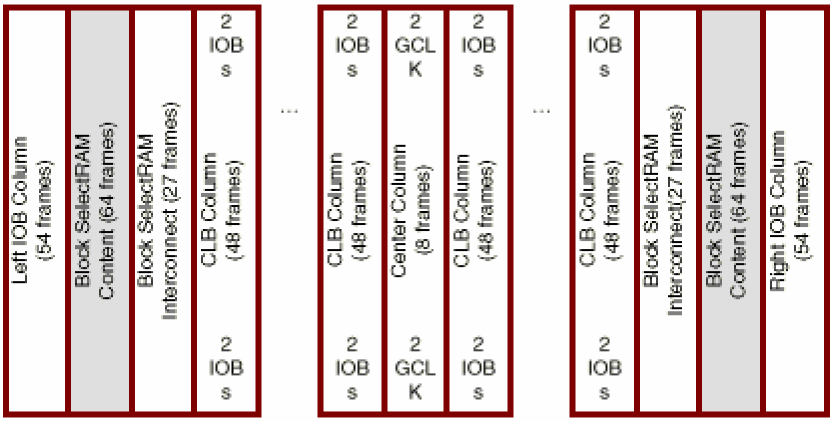


Figure 9.13 – Configuration column example

The address space (BRAM frames and CLB frames) is divided in Major and Minor addresses. The BRAM frames contain only the B*lock SelectRAM content* columns. The CLB frames contain all other column types. Each configuration column has a unique Major address within the RAM or CLB. Each configuration frame has a unique minor address within its column. Consequently, a frame address is expressed as a major address and a minor address.

Figure 9.14 exemplifies the columns in a Virtex device with the Major addresses. The shaded columns are in the RAM address space.

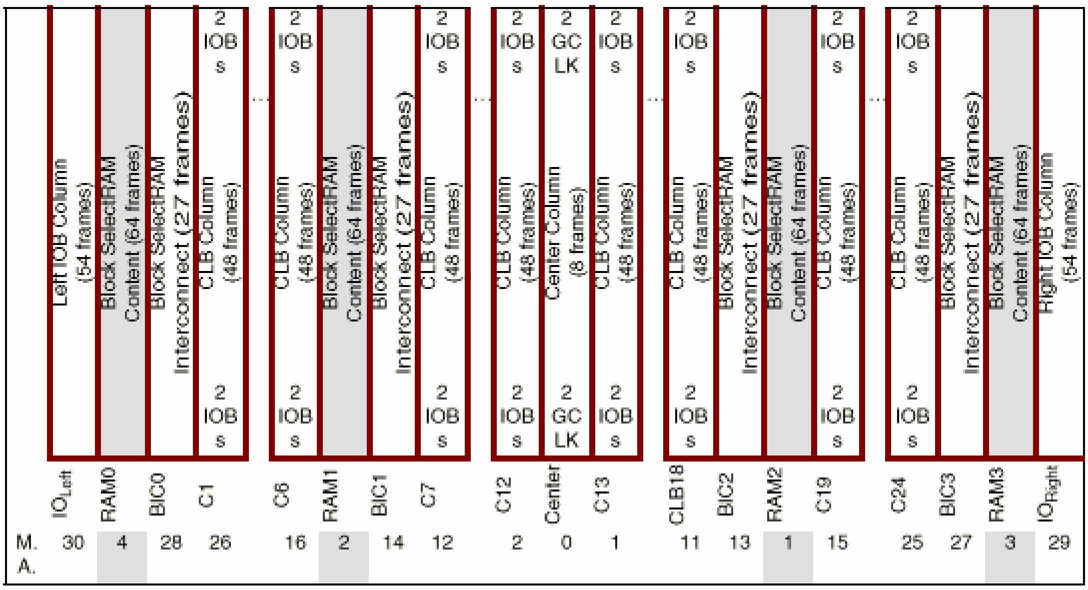
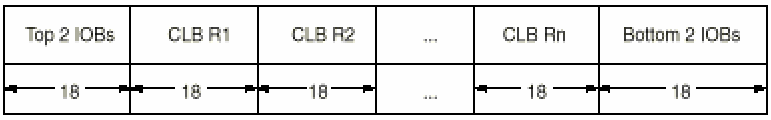


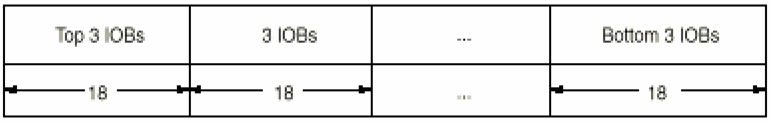
Figure 9.14 – Allocation of frames to device resources

The frame are read and written sequential with ascending address for each operation. The frame size depends on the number of rows in the device. The number of configuration bits in a frame is 18 x (# of CLB rows +2) and is padded with zeros on the right (bottom) to fit 32-bit word.

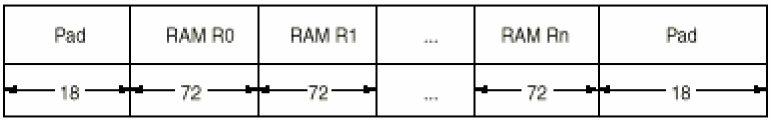
The frame organization differs to each type of column. Each frame is vertically in the device with the front of the frame at the top. However it is convenient to consider the frame horizontally when it is viewed as a part of a bitstream. The top is showed on the left. Figure 9.15 a, b and c show the CLB column frame, IOB column frame and Block SelectRAM content organization, respectively.



(a) CLB column frame



(b) IOB column frame



(c) Block SelectRAM content column frame

Figure 9.15 –Frame organization

The bits of a LUT SelectRAM are always spread across 16 consecutive frame Minor Addresses. With respect to the beginning of a configuration frame, relative locations of LUT SelectRAM bits within the bitstream are the same for every CLB slice. Each frame Minor Address contains all instances of a single bit index for that column. These 16 frames contain all 16 bits of the LUT SelectRAM for a column of CLB slices. It is necessary to read or write the 16 frames containing those bits to read or write the entire LUT SelectRAM. More information about the configuration architecture can be founded in the reference [XIL00b].

The SEU correction methods using the partial configuration capability are:

- *Readback:* SEU detection and single frame correction. In this case almost all the time the configuration logic will be at the read-mode. When an error is detected the effected frame must be corrected. This correct frame is written for a short period of time. Using readback for SEU detection requires a hardware implementation of algorithms for reading and evaluating each data frame. Additionally, memory space is needed to store constants and variables. The extra hardware must be SEU hardened.
- *Scrubbing*: reload the entire CLB frame segment at a chosen interval. This method reduces substantially the overhead in the system, but does mean that the configuration logic is likely to be in the write-mode for a great percentage of time.

9.1.3.1 Readback and Comparison

The more traditional method of verification of the data stored in configuration memory is to readback the data and to perform a bit for bit comparison. This requires the use of a mask file (.msk) and readback file (.rbb) each of which are equal in size to the original bit-stream used to configure the FPGA. Figure 9.16 shows an example of the data stream.

In some FPGAs the mask file can be very big. However, for space applications where memory is expensive and board space is substantial, storage of an extra 6.5 million bits is greatly undesirable. Therefore, a more efficient means is required. One solution is to reduce this mask file using an algorithm embedded in the configuration and readback controller, and to reduce the actual bitstream with a compression algorithm. The time necessary for correction depends of the FPGA size and this time can be dramatically reduced by the use of partial configuration.

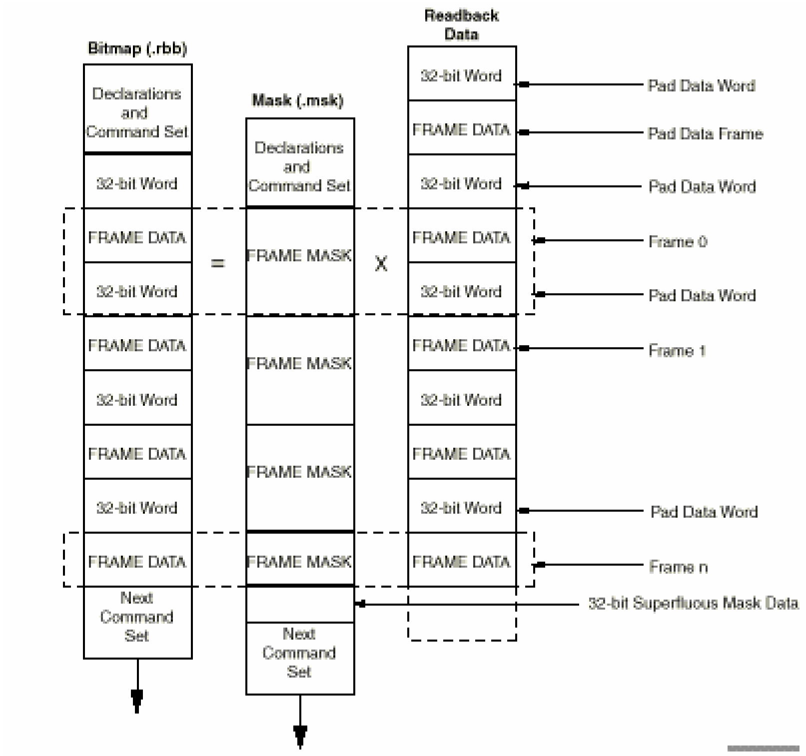


Figure 9.16 – Readback data stream alignment

The Los Alamos National Laboratories Space Data Systems Group [XIL00b] has developed another method for readback verification and SEU detection. This method records a 16-bit CRC (Cyclic Redundancy Check) value for each data frame. During readback a new CRC value is generated for each data-frame that is read back and compared to the expected CRC result. Since a data-frame is the smallest amount of configuration memory, which may be read from, or written to, the device, it is not important, to know which data bit is upset but merely which data frame the upset exists in. Then only the data frame effected need be rewritten to the FPGA to correct the SEU. This method greatly reduces the amount of system memory required to perform SEU detection.

The block diagram shown in figure 9.17 and 9.18 illustrate a readback CRC (Cyclic Redundancy Check) compare function easily implemented using a micro-controller. The micro-controller extracts the checksum from the readback serial stream and then compares it to the expected value. The output of the circuit, SEU_EVENT, can be used to interrupt to the system's processor signaling the occurrence of an SEU. At the next "convenient" time, the FPGA should be commanded to reconfigure.

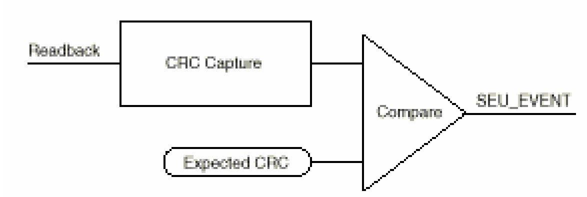


Figure 9.17 –Readback CRC comparator

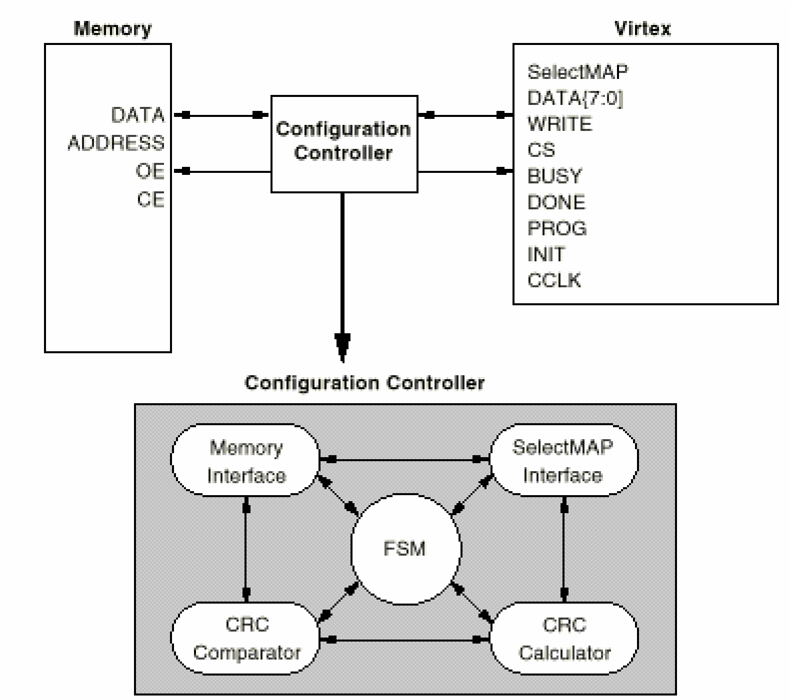


Figure 9.18 –Simple configuration and SEU correction design

9.1.3.1 Scrubbing

Scrubbing is a much simpler approach to SEU correction because it does not require any readback or data verification operations, nor does it require any data generation when reloading the data frames. In short, the process is to reload the bit-stream starting at the beginning, but stopping at the end of the first write to the frame data register (FDRI). In a standard bit-stream the first write to the FDRI register includes all the configuration data for the CLB Frames segment of the memory map. The rest of the bit-stream contains the BRAM segments, a CRC check, and the start-up sequence, all of which are not applicable to partial reconfiguration. No adjustments to the data or headers are needed.

The example shown in figure 9.19 demonstrates the use of a parallel (8-bit wide) memory device. This allows the data signals to be connected directly from the memory to the Virtex SelectMAP data pins. If the memory's data ports are of any other configuration then the data should be reorganized into 8-bit words within the control chip. For this example a simple counter is a sufficient state machine to control the scrubbing operations. The LSB outputs of the counter (number depends on the size of the memory) may be used as the address for the memory module. The example uses an 18-bit counter because this is the minimum value for a Virtex300 bit-stream. A Virtex600 or Virtex1000 would require a larger counter. Additionally, the system clock may be too fast for the configuration interface (50 MHz max). In which case the address lines could be shifted to higher order bits of the count value leaving the lower order bits to serve as a clock divider.

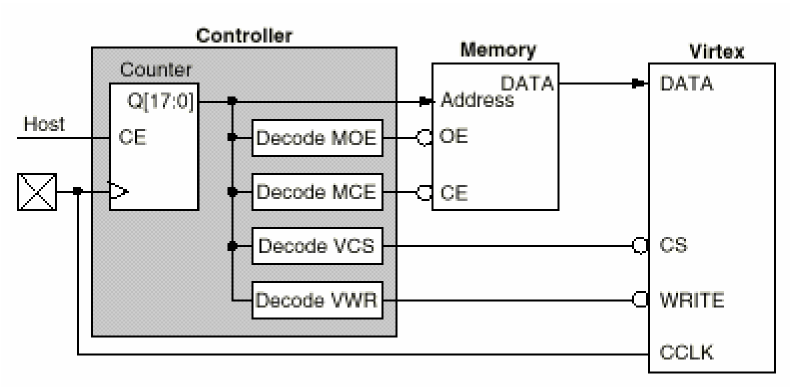


Figure 9.19 –Scrubbing control system

The scrub rate determines how often a scrub cycle should occur. The scrub rate should be determined by the expected upset rate of the device for the given application. For example, lets compare a 6,000 flip-flop ASIC to a 6,000 flip-flop Virtex Series FPGA. If the ASIC and the FPGA have similar process geometry, then the static cross-section per bit will be similar for both devices. However, the device cross-section is the bit cross-section multiplied by the number of bits in the device. For a 6000 flip-flop ASIC the number of bits is 6000, but for a Virtex FPGA this number is 6000 plus 1.7 Million (approximately) [XIL00b]. However, for an ASIC, a bit upset is considered to be a definite functional bit error. This would be an incorrect assumption for an FPGA. An upset in the configuration memory may or may not have any effect on the functional integrity of the user's design in the FPGA. This fact justifies the use of dynamic upset rate in FPGAs.

In [XIL00b], it is proposed a scrub rate, on average, ten times between upsets. For example, if we were to assume a bit upset rate of once per hour and a configuration clock frequency of 10 MHz, then the scrub rate should be once every six minutes.

<u>*SRAM-based FPGAs Resume*</u>*: In SRAM based FPGAs the combinational and sequential logic are SEU sensitive because RAM cells implement both of them. The only solution for SEU mitigation without changing matrix architecture is the logic redundancy or the bitstream reconfiguration. The logic redundancy can not correct upsets, consequently*

upsets can accumulate provoking error in the system. For applications that can be out of work for some seconds, the reconfiguration of the bitstream can be applied in FPGAs. This solution is to monitor the FPGA bitstream and if some error is detected a new bitstream without error is stored in the matrix. In [WAN99] the SEU in combinational and sequential logic in a FPGA matrix composed of SRAM memory is addressed. Solution using the DICE memory cells, presented in section 6, resistor memory cells and EDAC techniques are proposed. SRAM based FPGAs (Xilinx XC4000 series) show a low sensitive for atmosphere neutrons. Results shows that these SRAM based FPGAs can be used without limitation in the atmospheric radiation environment, contrary to large SRAM memories where precaution in the use is necessary because of neutron-induced SEU [LUM98], [FUL99].

9.2 SEU Mitigation Techniques for Anti-fused based FPGAs

In anti-fused based FPGAs the logic and the routing are determined by open or close anti-fuses that are consider to be fairly immune to radiation upsets. But the latch and flip-flops in anti-fused based devices are equally sensitive to radiation induced upsets as the latches in SRAM based FPGAs [KAT98].

The anti-fused based FPGAs have an advantage in terms of SEU mitigation compared to SRAM based FPGAs because the combinational logic part of a circuit implemented in the anti-fused based FPGA matrix uses the combinational part of the logic block instead of latches.

The most well known company that fabricates anti-fused based FPGAs is Actel [ACT98]. Its matrix is composed of rows of logic blocks and routing channels as it is shown in figure 9.20.

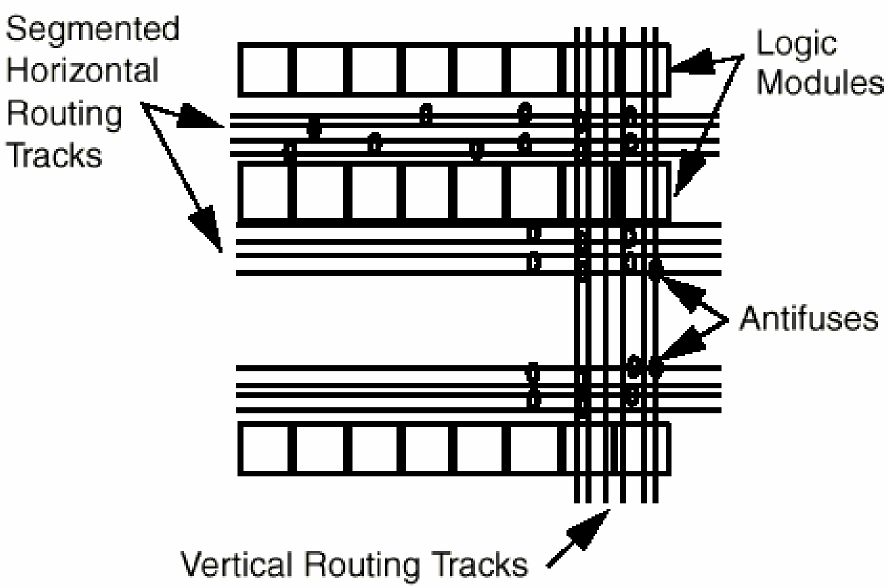


Figure 9.20 – Actel interconnection matrix

The programmable anti-fuses elements are illustrated in figure 9.21.

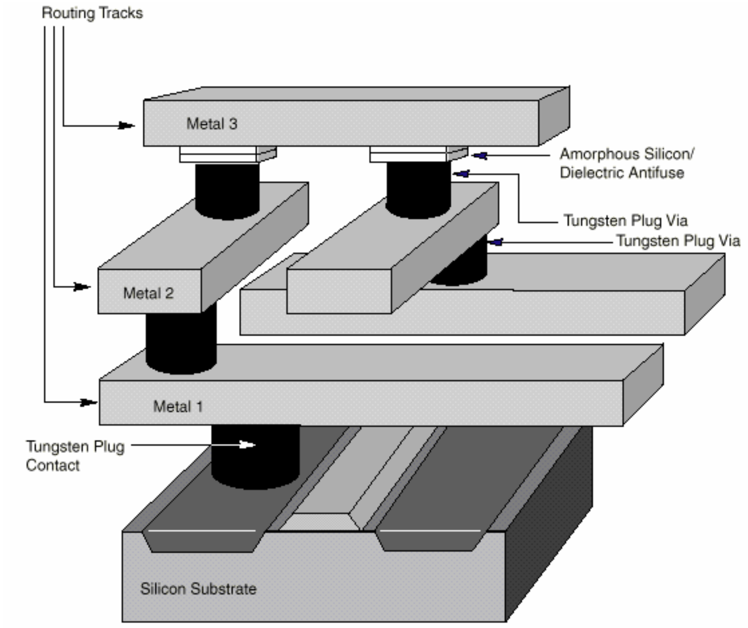


Figure 9.21 – Actel interconnections elements

The routing channels have been suppressed in the new technologies due to the high number of metal layers. The interconnection between the logic blocks is achieved using Actel's patented metal-to-metal programmable anti-fuse interconnect elements, which are embedded between the metal 2 and metal 3 layers. The anti-fuses are normally open circuit and, when programmed, form a permanent low-impedance connection. In this technique, there is no bit-stream to load into the FPGA.

There are two kinds of logic blocks in the Actel matrixes, combinational logic blocks (C-module) and sequential logic blocks (S-module). These blocks are showed in figure 9.22.

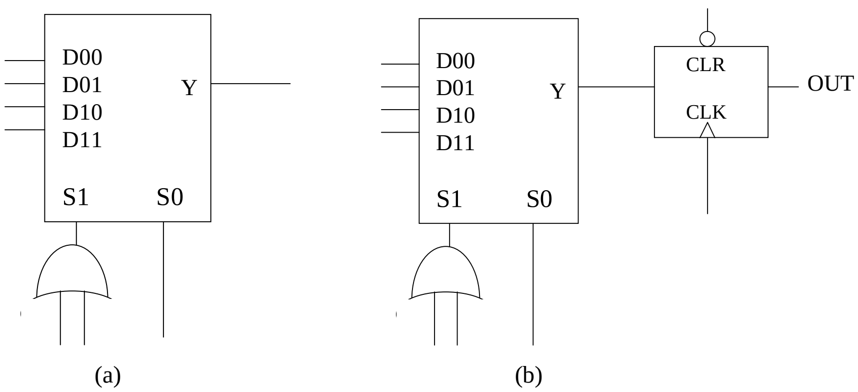


Figure 9.22 – Combinational ACT1 (a) and sequential ACT1 logic blocks

The S-module can implement the same combinational logic as the C-module, and it also contains a flip-flop that can be configured by different ways. This flip-flop is called SFF.

There are two hardened families from Actel: RH1280 and RH1020. Table 9.5 summarizes their characteristics.

Table 9.5 – Hardened FPGA families from Actel

Family	# Gates	# of C-modules	# of S-modules
RH1280	8,000	608	624
RH1020	2,000	547	0

The most sensitive elements of the Actel FPGA are the flip-flops from the S-modules. The error rate is $1x10^{-6}$ upsets per bit-day in a 90% worst case geosynchronous Earth orbit. These flip-flops must be protected to avoid upsets.

There are two techniques for SEU mitigation proposed by Actel. The first one is to avoid the use of the flip-flops in the FPGA matrix. In other words, the SFF in the S-module must be avoided. For this first solution two logic blocks using only the combinational logic parts of the logic blocks must implement a flip-flop in the system. The flip-flop can be constructed in four different ways: C-C, C-S, S-C and S-S modules. This solution has been called *bypassed S-module*.

The second proposed technique by Actel is to triplicate the implementation of a flip-flop in the matrix and to vote the write output. This solution is called triple modular redundancy (TMR). Figure 9.23 shows this method. This technique can significantly improve the SEU immunity; however the trade-off to using TMR is that it requires an increased amount of device resources.

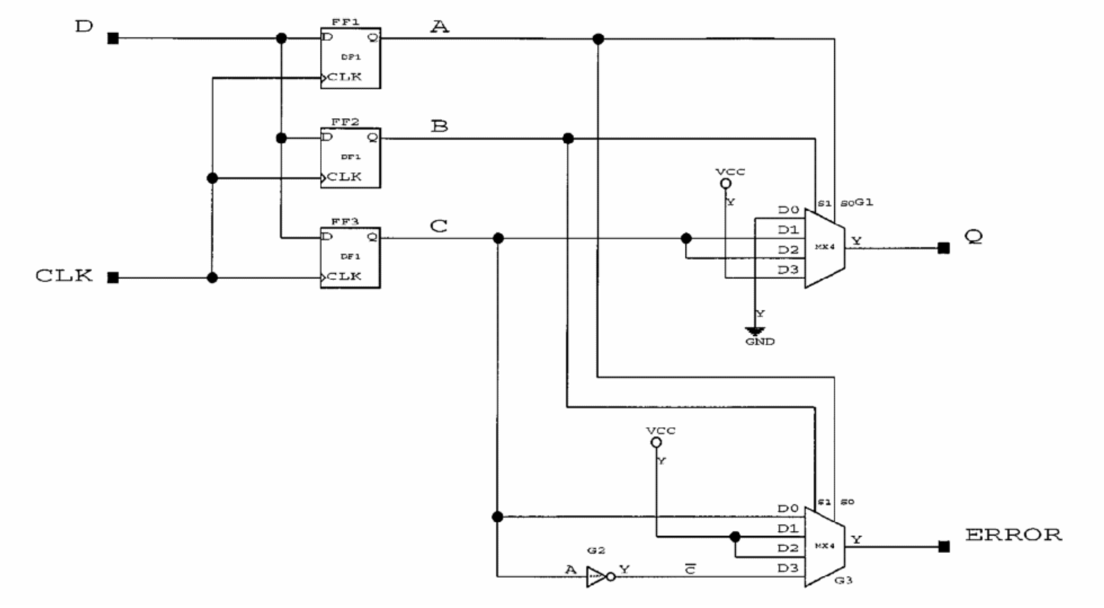


Figure 9.23 – Actel TMR implementation

For memory elements such as loadable registers, a modified TMR circuit, shown in figure 9.24, can be used. This circuit will constantly refresh itself by feeding corrected data back into the inputs of the flip-flops when the enable (E) input is low, permitting error-free data to be held indefinitely. When enable is high, new data is loaded into the TMR triplet. Again, this circuit very efficiently maps into the RH1280 architecture. Typically, this configuration requires only four logic modules if the SFFs are used.

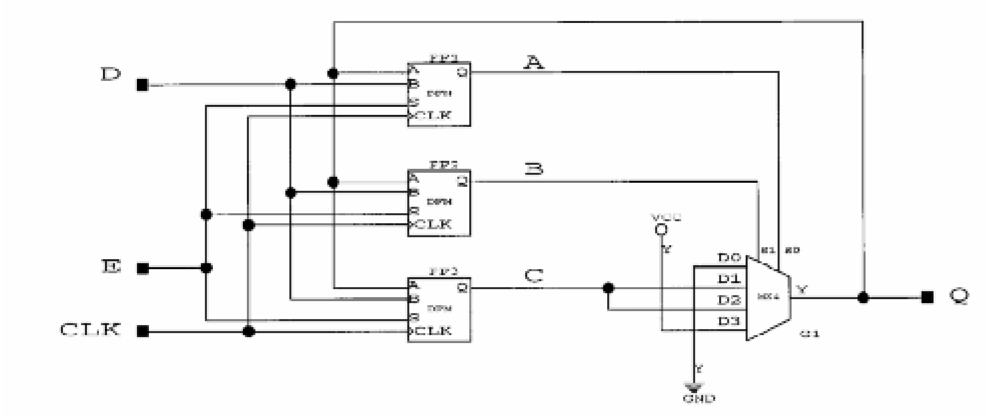


Figure 9.24 – Actel register element with TMR

A J-K flip-flop TMR circuit with refresh is shown in Figure 9.25. It operates on a similar principle to the circuit shown in figure 9.23, with the voter circuit inside the feedback loop. Each of the three 4:1 MUX and flip-flop pairs will map into one S-Module using the SFF. The voter MUX and inverter (for toggling) cannot be combined, resulting in a typical number of five modules per J-K flip-flop.

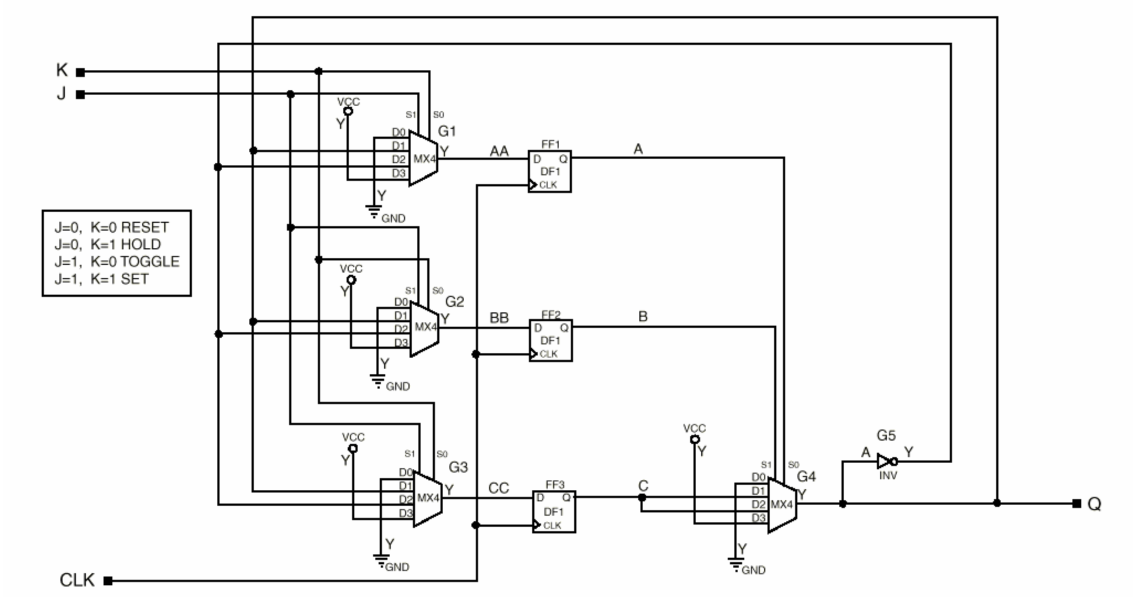


Figure 9.25 – Actel J-K flip-flop with TMR

<u>Anti-fuse FPGAs Resume</u>: *In anti-fused FPGAs it is possible to implement sequential logic using the combinational part of the logic blocks in the matrix. This can solve the problem of SEU in the memory elements. However, this solution reduces the area*

density in the matrix. To apply this solution it would be better to develop a matrix composed only of combinational logic bocks. Another potential solution is to triplicate the logic modules using TMR. But this method, like it was mentioned before, can not correct upsets and consequently upsets can accumulate provoking errors in the system. This approach also presents low area efficiency and can reduce the performance of the circuit.

9.3 SEU Mitigation Techniques for EPLDs

Programmable Logic Devices programmable by the EEPROM cells are called EPLDs because they can be electrically programmed. They differ from standard FPGAs in terms of matrix structure. The logic structure is based on arrays of OR/AND logic cells. Their performance and density are usually smaller compared to SRAM-based FPGAs.

Altera is one of the companies in the market to produce EPLDs. The families from Altera are named MAX. The families are composed of Logic array blocks (LABs), macrocells, expander product terms, fast track interconnects, and dedicated inputs and I/O blocks, as presented in figure 9.26.

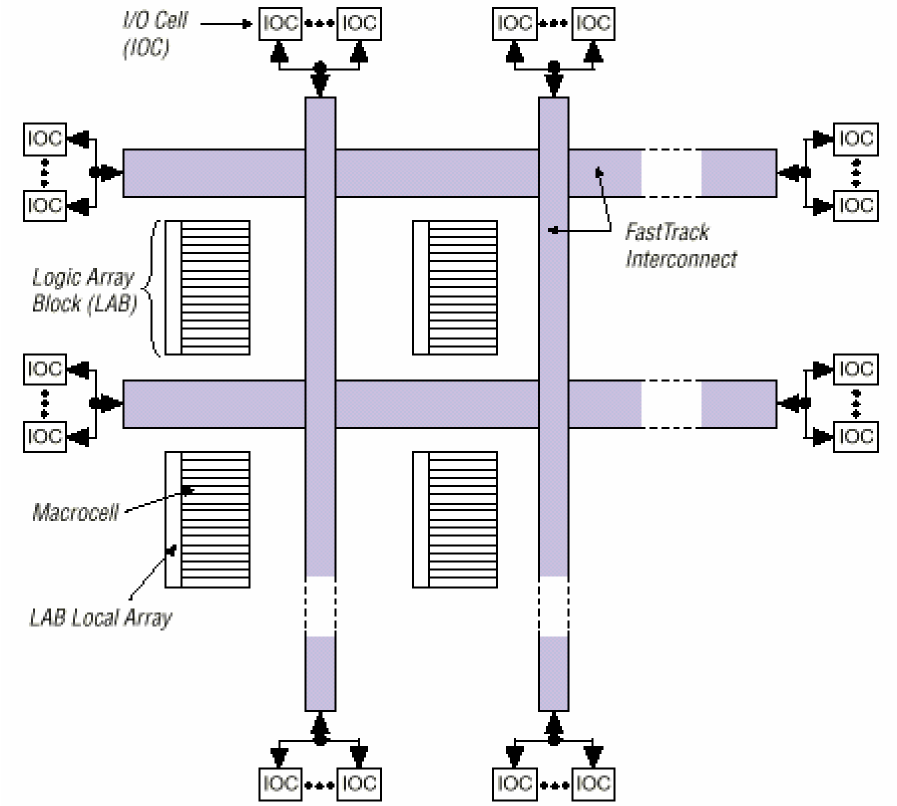


Figure 9.26 – MAX9000 device block diagram from Altera

MAX9000 EPLDs contain 320 to 560 macrocells that are combined into groups of 16 macrocells, called logic array blocks (LABs), figure 9.27. Each macrocell has a programmable AND / fixed OR array and a configurable register with independently clock, enable, etc… To build complex logic functions, each macrocell can be supplemented with both sharable expander product terms and high-speed expander product terms to provide up to 32 product terms per macrocell. The macrocell structure is illustrated in figure 9.28.

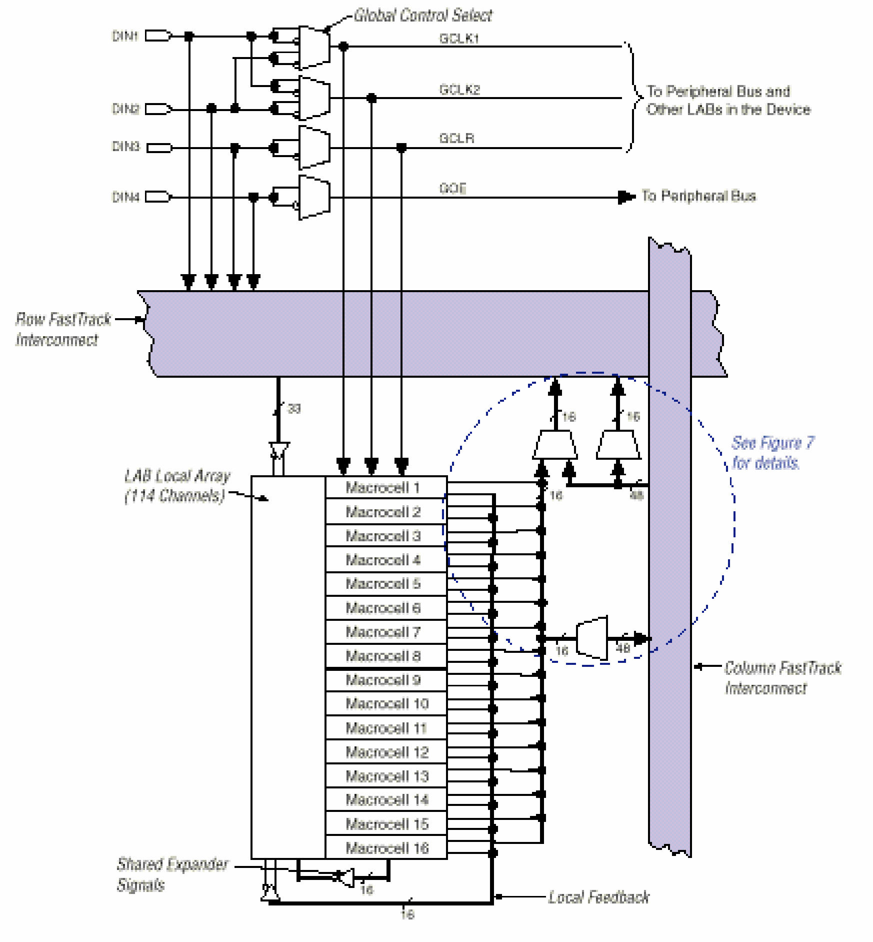


Figure 9.27 – MAX9000 logic array block from Altera

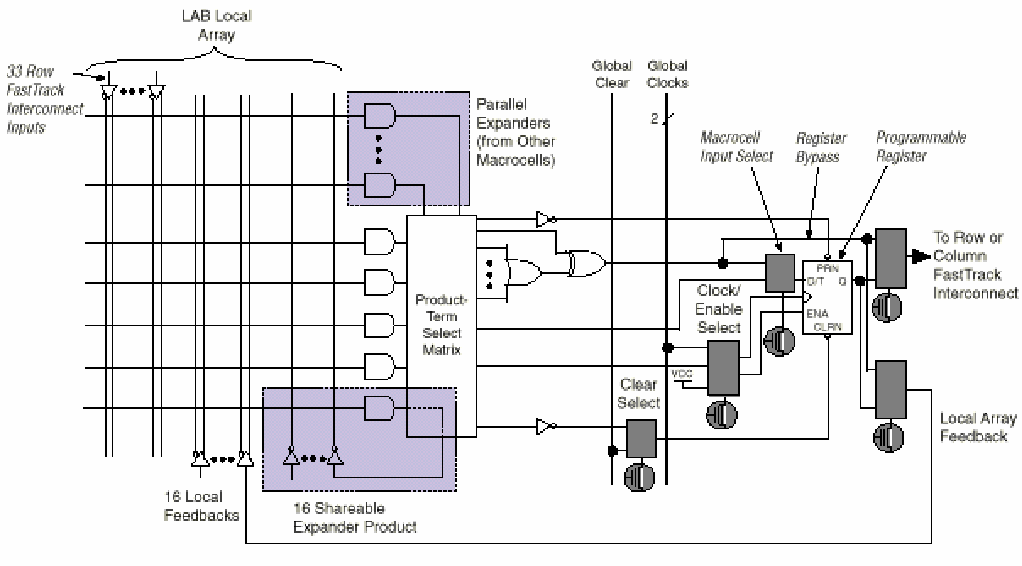


Figure 9.28 – MAX 9000 macrocell from Altera

There are no Hardened families of EPLDs proposed by Altera. In contrast, PLDs programmable by EEPROM have some advantages in the matrix structure in terms of radiation protection. The logic in the matrix is basically implemented using AND/OR logic. This logic by construction is not so SEU sensitive as memory cells presented, for example, in Lookup Tables (LUTs).

Aiming at protecting the EPLDs against SEU, it is necessary to apply some mitigation techniques in all memory cells and programmable elements (EEPROM). The memory cells can be affected by charged particles as it was presented before in this report. The transient pulse provoked by the hit can flip the value stored in the memory cell. The programmable element called EEPROM can be also affected by SEU because a charged particle hit can turn on or off the EEPROM transistor according to the amount of charge deposited by the hit. Figure 9.29 shows an example of EPROM transistor structure.

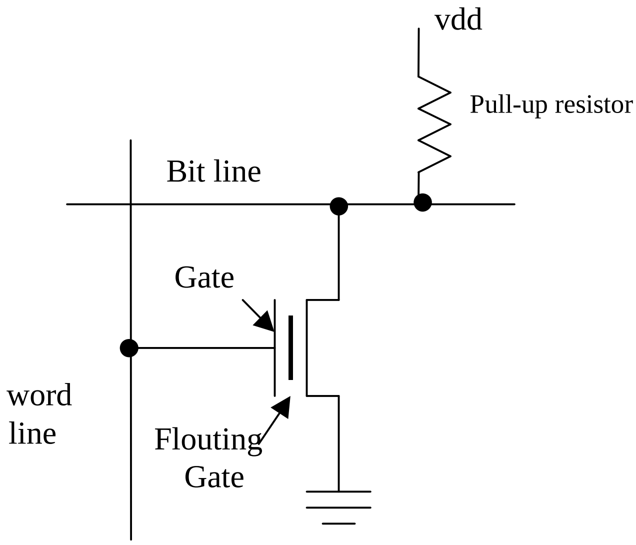


Figure 9.29 – EPROM transistor programmable element

The SEU mitigation techniques in the EEPROM element are based on the technology. The foundry must use a specific process to avoid or reduce the transient current generated by the charged particle hit.

<u>EPLDs Resume</u>: In EPLDs, the combinational logic is implemented in OR/AND arrays that are by construction immune to single event upsets. The sequential logic is implemented in memory cells that must be protected to avoid bit flip. The programmable logic elements are EPROM that must be built in an appropriated technology to be insensitive to radiation. No solutions to SEU mitigate EPLDs devices have been proposed yet by commercial manufactors.

.

10 Conclusion

Digital circuits designed for space applications must be tolerant to radiation. The charged particles presented in the radiation environment can provoke destructive and non-destructive effects. This work has focused a well-known non-destructive effect called Single Event Upset (SEU) that is characterized as a bit flip in memory cells that is generated by a single charged particle hit in a circuit silicon surface. Aiming at mitigating this kind of error, some solutions have been developed in the last few years. However until now, there is no completely successful and general solution to mitigate SEU in integrated circuits and systems.

This report has addressed protection methodologies used nowadays for digital designs that can achieve satisfied reliability for space applications. The SEU mitigate solutions on digital circuits can be done by different approaches: hardening by technology, hardening by design and hardening by system.

In hardening by technology, the integrated circuits are fabricated using a special SEU hardened process technology such as SOI technology process. The main drawback of this approach is the cost. Due to the low volume level of devices in hardened technology process, the chips are much more expensive and usually use older technologies compared to COTS circuits. However IBM has stated that it will implement silicon-on-insulator (SOI) technology in volume by the end of this year. IBM expects SOI will eventually replace bulk CMOS as the most commonly used substrate for advanced CMOS in mainstream microprocessors and other emerging wireless electronic devices requiring low power. Using SOI technology for digital circuits, SEU sensibility is dramatically reduced and in some cases it allows to manufacture circuits immune to the effects of radiation. One of the main advantages of SOI is a very good performance at low-voltage operation for reduce chip's power consumption.

In hardening by design, the standard CMOS technology process is maintained for space applications to reduce the device cost. SEU hardened memory cells are developed using feedback elements. This solution has a great advantage because it can provide SEU hardened memory in COTS technology. This solution is suitable to ASICs design projects as well as to develop specific gate array matrix. This work has showed some SEU hardened memory cells in the section 6. All presented hardened memory cells are based on duplication and feedback approaches. They differ from each other in terms of number of transistors, performance and SEU immunity degrees. The basic idea is to add transistors in the standard memory cell with an appropriated feedback devoted to restore the data corrupted by an ion hit. An careful analysis of the characteristics of the presented hardened memory cells, the DICE cell presents one of the best solutions for logic circuits according to area, performance and immunity.

In hardening by system, modifications in the circuit implementation are adopted to turn the device SEU immune. A typical mitigation solution at the system level is called Triplicate Modular Redundancy (TMR) that consist to triplicate all the memory parts of the system and to choose the correct data using a voter. This method can be used for ASICs and for programmable circuits.

Due to the large use of FPGAs in space projects, mainly for re-configurable applications, solutions to mitigate SEU in programmable logic devices are becoming meaningful. FPGA manufactures proposes the triple modular redundancy with voter (TMR) to reduce the SEU sensitivity. However, this technique increases the area and the performance of the circuit. Moreover, upset faults detected by the TMR can not be corrected by the system, although additional logic is included to correct the faults.

An alternative SEU mitigation solution for FPGAs is to replace all the memory cells in the FPGA architecture to SEU hardened memory cells. However this solution requires a new design project of the matrix and consequently it is very costly in terms of development and time.

The protection technique of a digital circuit can be also performed in a high level description, for example in VHDL. In this case the project can be implemented in a programmable device or in an ASIC using some special libraries that make the high description SEU immune. This solution has a great advantage for FPGAs devices because it may need less logic blocks for the circuit implementation than the TMR solution avoiding thus modifications in the FPGA matrix. This solution can be optimized in terms of area, performance and power, improving the SEU hardened circuit. However it does not solve completely the FPGA radiation sensibility, meanly in SRAM-based FPGAs where all the combinational logic and connections are SEU sensitive.

In the near future, due to the constantly progress in CMOS technologies which lead to decreasing transistors features (gate dimensions and voltage supplies), the neutron particles presented in the atmosphere will be able to affect digital logic circuits operating on ground applications [NOR96], [OHL97]. This problem may be concern digital logic device developments to avoid upsets in the functionality in both combinational and sequential logic. For example, combinational logic can be protected against SEU using Canaris approach [WIS93] based on complex logic cells.

There are still now many researches to do in terms of radiation protection of digital circuits. New solutions must be proposed in the next years in order to meet the necessities of the market such as performance, power, cost and turnaround time.

References

[ACT98] ACTEL. Design Techniques for Radiation-Hardened FPGAs. Application Note. In: http://www.actel.com (Sep. 1997).

[ALF98] ALFKE, Peter; PADOVANI, Rick. Radiation Tolerance on High-Density FPGAs. In: http://www.xilinx.com (Oct. 1998).

[ALT98] ALTERA CORPORATION. Data Sheet. Disponível por WWW em http://www.altera.com (nov. 1998).

[BAR97] BARTH, Janet. Radiation Environment. In: IEEE NSREC Short Course, July 21, 1997. http://flick.gsfc.nasa.gov/radhome/ RPO_slides.htm.

[BES93] BESSOT, Denis. Conception de Deux Points Memoire Statiques CMOS durcis Contre L'effet des Aleas Logiques Provoques par L'environment Radiatif Spatial. These. INPG. Novembre, 1993.

[BRY98] O'BRYAN, Martha; LABEL, Kenneth A.; REED, Robert A; BARTH, Janet; SEIDLECK, C.; MARSHALL, Paul; MARSHALL, C.; CARTS, Martin. Single Event Effect and Radiation Damage Results For Candidate Spacecraft. In: IEEE NSREC Conference, 1998.

[CAL96a] CALIN, T.; VELAZCO, R.; NICOLAIDIS, M.; MOSS, S; LAMONDIERE, S. D.; TRAN, V. T.; KOGA, R. Topology-Related Upset Mechanisms in Design Hardened Storage Cells. In: NSREC Conference, 1996.

[CAL96b] CALIN, T.; NICOLAIDIS, M.; VELAZCO, R. Upset Hardened Memory Design for Submicron CMOS Technology. In: IEEE Transactions on Nuclear Science. VOL. 43, NO. 6, December 1996.

[CAM99] CARMICHAEL, C.; FULLER, E.; BLAIN, P.; CAFFREY, M. SEU Mitigation Techniques for Virtex FPGAs in Space Applications. In: http://www.xilinx.com (Sep. 1999).

[CAR96] CARRO, L.; PEREIRA, G.; SUZIN, A. Prototyping and Reengineering of Microcontroller-Based Systems. In: IEEE Rapid Systems Prototyping Workshop. Proceedings… June 1996.

[CHI98] CHIP EXPRESS CORPORATION. Data Sheet. Disponível por WWW em http://www.chipexpress.com (nov. 1998).

[COT00] COTA, E.; CARRO, L.; LUBASZEWSKI, M.; VELAZCO, R.; REZGUI, S. Synthesis of 8051-like Microcontroller Tolerant to Transient Faults. In: 1st IEEE Latin America Test Workshop (LATW), Brazil, 2000.

[DEN00] Martin Dentan. RADIATION EFFECTS ON ELECTRONIC COMPONENTS AND CIRCUITS. In: CERN Training Course. April 11, 2000. (http://atlas.web.cern.ch/Atlas/GROUPS/FRONTEND /radhard.htm).

[DON93] DONG, S. K. et al. Two channel Routing Algorithms for Quick Customized Logic. In: EDAC, 1993. Proceedings… Los Alamitos : IEEE Computer Society, 1993. p. 122-126.

[FUL99] FULLER, E.; BLAIN, P.; CAFFREY, M.; CARMICHAEL, C. Radiation Test Results of the Virtex FPGA and ZBT SRAM for Space Based Reconfigurable Computing. In: http://www.xilinx.com (Sep. 1999).

[IBM00] IBM. SOI Technology: IBM's Next Advance in Chip Design. In: http://www.ibm.com (Jan. 2000).

[HOP99] HOPKIN, Vince. Programmable Device or Gate Array? Disponível por WWW em http://www.isdmag.com (jan., 1999).

[KAT94] KATZ, R.; BARTO, R.; McKERRACHER, P.; CARKHUFF, B; KOGA, R. SEU Hardening of Field Programmable Gate Arrays (FPGAs) for Space Application and device characterization. In: NSREC Conference, 1994.

[KAT97] KATZ, R.; LABEL, K.; WANG, J.; CRONQUIST, B.; KOGA, R.; PENZIN, S.; SWIFT, G. Radiation Effects on Current Field Programmable Technologies. In: NSREC Conference, 1997.

[KAT98] KATZ, R.; WANG, J.; LABEL, K.; McCOLLUM, J.; BROWN, R.; REED, R.; CRONQUIST, B.; CRAIN, S.; SCOTT, T.; PAOLINI, W.; SIN, B. Current Radiation Issues for Programmable Elements and Devices. In: NSREC Conference, 1998.

[LAB99] LABEL, K. et al. Commercial Microelectronics Technologies for Applications in the Satellite Radiation Environment. In: http://flick.gsfc.nasa.gov/ radhome.htm (Nov. 1999).

[LIU92] LIU, M.; WHITAKER, S. Low Power SEU immune CMOS Memory Circuits. In: NSREC Workshop. 1992.

[LIM98] LIMA, Fernanda G.; CARRO, Luigi; GUNTZEL, José Luís; JOHANN, Marcelo de O.; REIS, Ricardo. Improving Logic Density of QCL Masterslices by Using Universal Logic Gates, In: SBCCI, 1998, Buzios, Brasil.

[LIM99] LIMA, Fernanda G.; JOHANN, Marcelo; GUNTZEL, José Luiz; DAVILA, Eduardo; CARRO, Luigi; REIS, Ricardo. Designing a Mask Programmable Matrix for Sequential Circuits. In: VLSI Conference, 1999, Lisboa, Portugal.

[LIM00] LIMA, Fernanda G.; COTA, Érika; CARRO, Luigi; LUBASZEWSKI, Marcelo; REIS, Ricardo; VELAZCO, Raoul; REZGUI, Sana. Designing a Radiation Hardened 8051-like Micro-controller. In: SBCCI Conference. Proceedings…, 2000.

[LUM98] LUM, G.; MARTIN, L. Single Event Effects Testing of Xilinx FPGAs. In: http://www.xilinx.com (Oct. 1998)

[NOR96] NORMAND, Eugene. Single Event Upset at Ground Level. In: IEEE Transactions on Nuclear Science. VOL. 43, NO. 6, December 1996.

[OHL97] OHLSSON, M.; DYREKLEV, P.; JOHANSSON, K.; ALFKE, P. Neutron Single Event Upsets in SRAM based FPGAs. In: http://www.xilinx.com (1997).

[PET80] PETERSON, W. Wesley. Error-correcting codes. Ed. 2.ed. Cambridge : The mit Press, 1980. 560 p. ISBN 0262160390.

[PLA00] PLANK, James S. A Tutorial on Reed-Solomon Coding for Fault-Tolerance in RAID-like Systems. Department of Computer Science, University of Tennessee. In: http:// www.cs.utk.edu/~plank/plank/papers/SPE-9-97.html

[RAB96] RABAEY, Jan. Digital Integrated Circuits - A Design Perspective. Upper Saddle River : Prentice Hall, 1996. 702 p.

[REZ00] REZGUI, S.; VELAZCO, R.; ECOFFET, R.; RODRIGUEZ, S; MINGO, J. R. Estimating Error Rates in Processor-Based Architectures. In: RADECS Workshop, 2000.

[RIT99] RITTER, James. Microelectronics and Photonics Test Bed. In: http://ssdd.nrl.navy.mil/www/mptb/introduction.htlmx (Nov. 1999).

[ROC92] ROCKETT, L. SEU Hardened Scaled CMOS SRAM Cell Design Using Gate Resistors. In: IEEE Transactions on Nuclear Science. October, 1992.

[STA88] STASSINOPOULOS, E.; RAYMOND, J. The Space Radiation Environment for Electronics. In: Proceedings of the IEEE, VOL. 76, NO. 11, November 1988.

[VEL94] VELAZCO, R.; BESSOT, D.; DUZELLIR, S.; ECOFFET, R.; KOGA, R. Two Memory Cells Suitable for the Design of SEU-Tolerant VLSI Circuits. In: IEEE Transactions on Nuclear Science. VOL. 41, NO. 6, December 1994.

[VEL98] VELAZCO, R; REZGUI, S.; CHEYNET, Ph.; BOFILL, A.; ECOFFET, R. THESIC: A Testbed suitable for the qualification of integrated circuits devoted to operate in harsh environment. In: IEEE European Test Workshop (ETW'98) pp. 89-90, 27-29 Mai 1998, Spain.

[VEL00] VELAZCO, R.; REZGUI, S.; ECOFFET, R. Transient bitflip injection on microprocessor-based digital architectures, presented at Nuclear and Space Radiation Effects Conference, NSREC 2000 , (Reno, USA, 24-29 July 2000).

[WAN99] WANG, J.; KATZ, R.; CRONQUIST, B.; MCCOLLUM, J.; SPEERS, T.; PLANTS, W. SRAM Based Re-programmable FPGA for Space Application. In: NSREC, 1999.

[WEA87] WEAVER, H.; et al. An SEU Tolerant Memory Cell Derived from Fundamental Studies of SEU Mechanisms in SRAM. In: IEEE Transactions on Nuclear Science. VOL. 34, NO. 6, December 1987.

[WHI91] WHITAKER, S.; CANARIS, J.; LIU, K. SEU Hardened Memory Cells for CCSDS REED Solomon Encoder. In**:** IEEE Transactions on Nuclear Science. VOL. 38, NO. 6, December, 1991.

[SIA94] *Sia* Semiconductor Industry Association. The National Technology Roadmap for Semiconductors. 1994.

[SKA96] SKAHILL, Kevin. VHDL for Programmable Logic. [S.l.] : Addison Wesley. 1996, p. 1-23.

[WIS93] WISEMAN, D.; CANARIS, J.; WHITAKER, S.; VEMBRUX, J.; CAMERON, K.; ARAVE, K.; ARAVE, L.; LIU, N.; LIU, K. Design and Testing of SEU / SEL Immune Memory and Logic Circuits in a Commercial CMOS Process. In: NSREC Conference, 1993

[XIL00a] XILINX CORPORATION. Devices Data Sheet. In: http://www.xilinx.com. (Nov. 2000).

[XIL00b] XILINX CORPORATION. Aerospace and Defense Programmable Logic Data Sheet 2000. In: http://www.xilinx.com/products/hardwire/hardwirehome.htm (Sept. 2000).