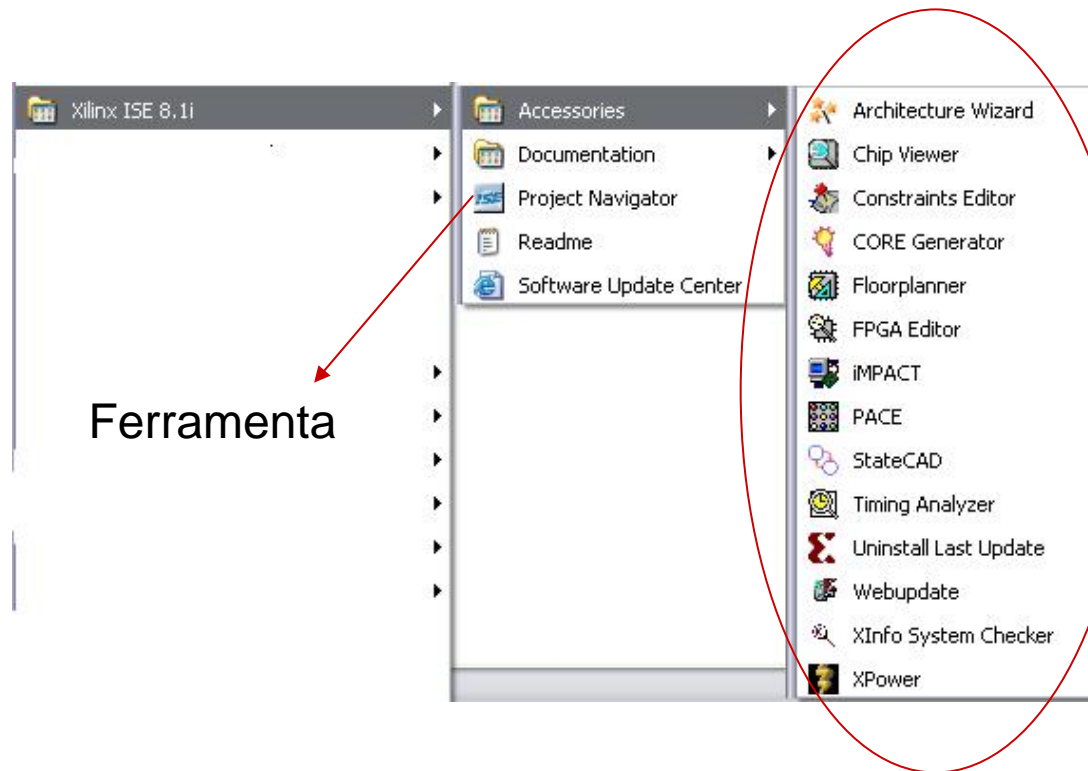




# Tutorial ISE

- Descrição esquemático
- Descrição Máquina de Estados
- Síntese
- Simulação

- [www.xilinx.com](http://www.xilinx.com) (documentação)



Ferramenta

Ferramentas auxiliares que podem ser chamadas de dentro do Project Navigator

# Passo 1: Criar um novo projeto

ISE New Project Wizard - Create New Project

Enter a Name and Location for the Project

Project Name:

Project Location: JAS-INFAPLIC-2005-ATUAL\istemas\_digitais\WHDL\

Select the Type of Top-Level Source for the Project

Top-Level Source Type: Schematic

More Info < Back Next > Cancel

Escolher entre:  
- Esquemático  
- HDL

# Passo 2: Escolher FPGA e ferramentas

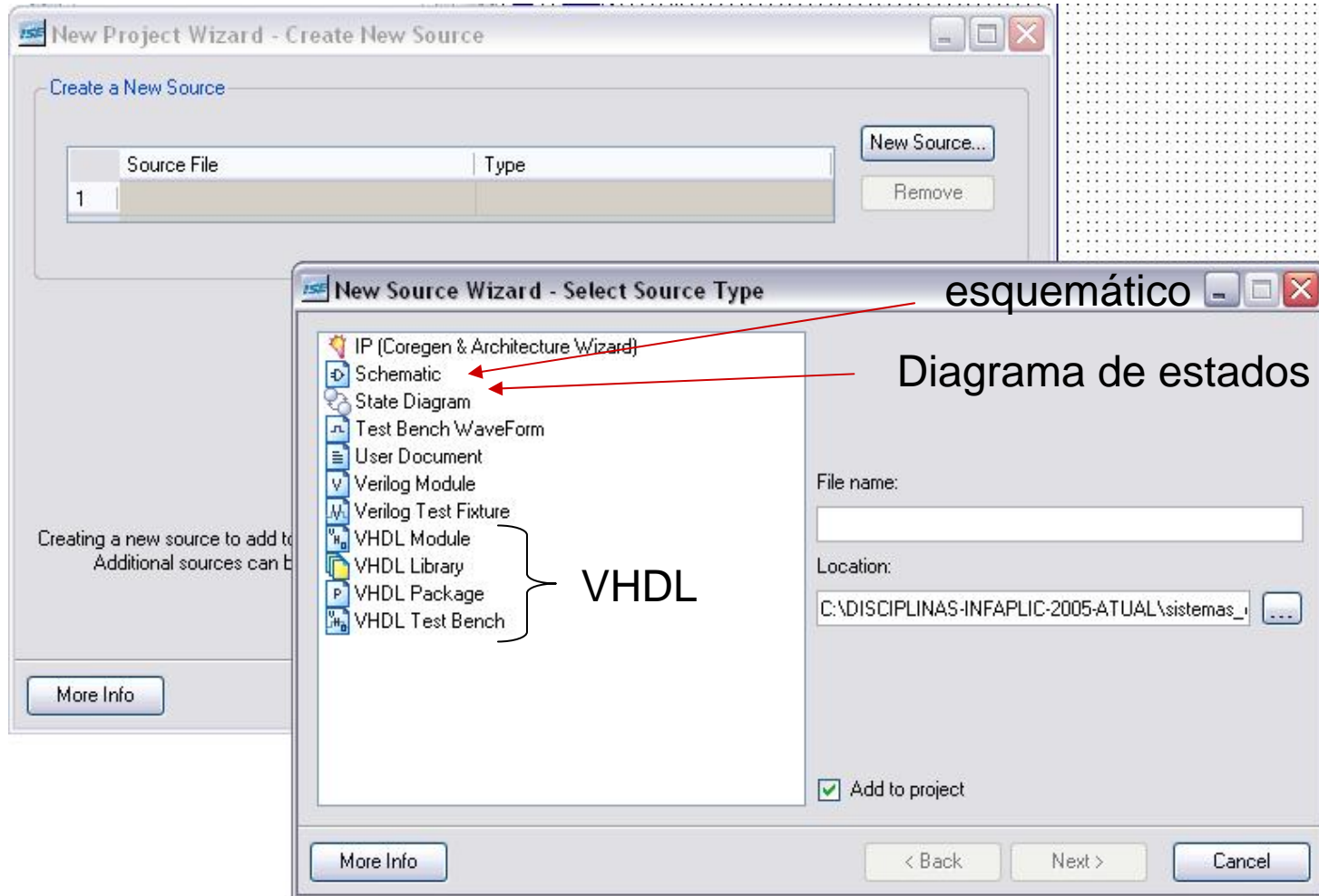
Property Name	Value
Product Category	All
Family	Spartan3
Device	XC3S200
Package	PQ208
Speed	-5
Top-Level Source Type	Schematic
Synthesis Tool	XST (VHDL/Verilog)
Simulator	ISE Simulator (VHDL/Verilog)
Enable Enhanced Design Summary	<input checked="" type="checkbox"/>
Enable Message Filtering	<input type="checkbox"/>
Display Incremental Messages	<input type="checkbox"/>

Escolher a família e o FPGA

encapsulamento

Ferramentas de síntese e o simulador

# Passo 3: Criar um novo circuito (fonte)



## Inserir instancias e portas no esquemático

The screenshot displays the Xilinx ISE software interface. The main workspace shows a schematic diagram of a digital circuit with logic gates (XOR, AND, OR) and a sum output. The 'Sources' window on the left shows the project structure, with 'somador1bit (somador1bit.sch)' selected. The 'Processes' window, highlighted with a red border, lists various tasks, with 'Generate Programming File' selected. A red oval highlights the 'Synthesis/Implementation' folder in the Sources window. A red arrow points from the 'Generate Programming File' process to the console window at the bottom, which displays the message: 'Started : "Generate Programming File". Process "Generate Programming File" completed successfully'. The console window also shows tabs for 'Console', 'Errors', 'Warnings', and 'Find in Files'. The status bar at the bottom indicates 'Ready' and 'T2552.5001'.

Janela dos processos

Circuito inserido no projeto (botão da direita do mouse para inserir novos arquivos)

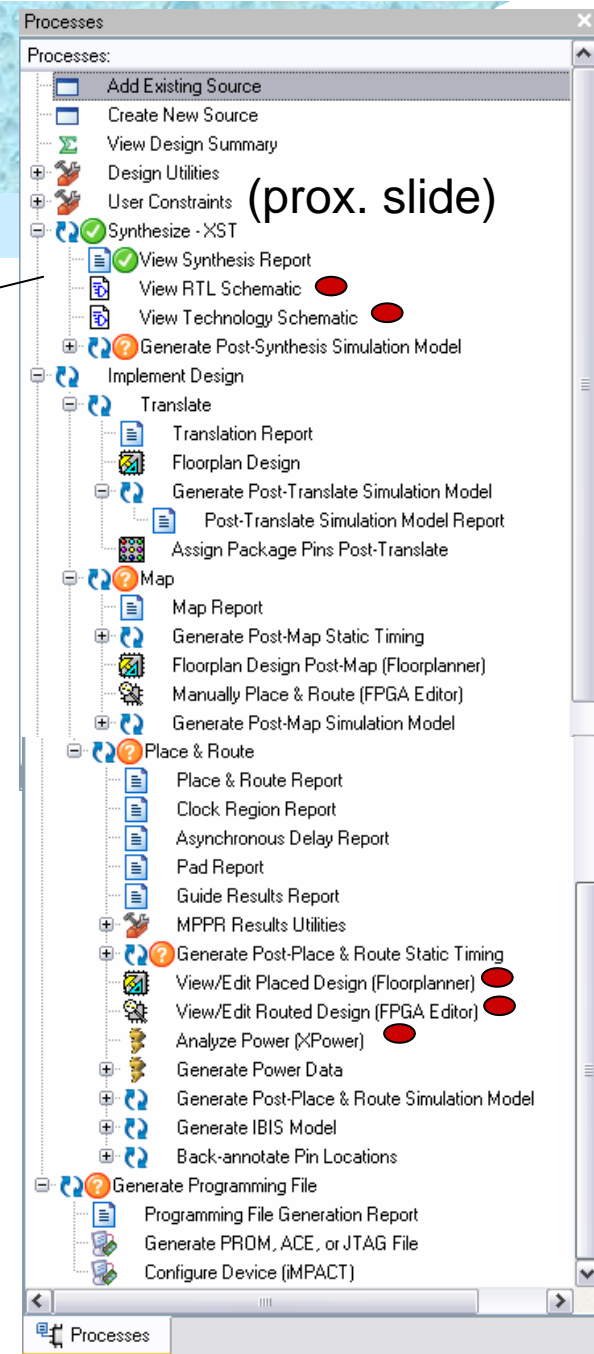
# Analizando os processos

Síntese inicial  
(mapeamento para  
biblioteca padrão de  
nands e nors)

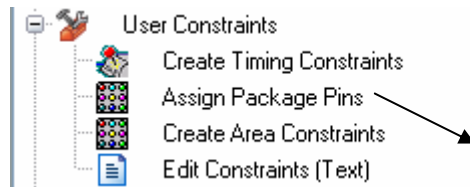
Todo o processo tem propriedades que podem ser configuradas (basta apertar o botão da direita do mouse em cima do processo).

Para rodar um processo basta apertar RUN (usando o botão da direita do mouse ou double click)

- Todas estes processos ao fazer um “double click” uma nova janela irá abrir mostrando o resultado ou nova ferramenta.

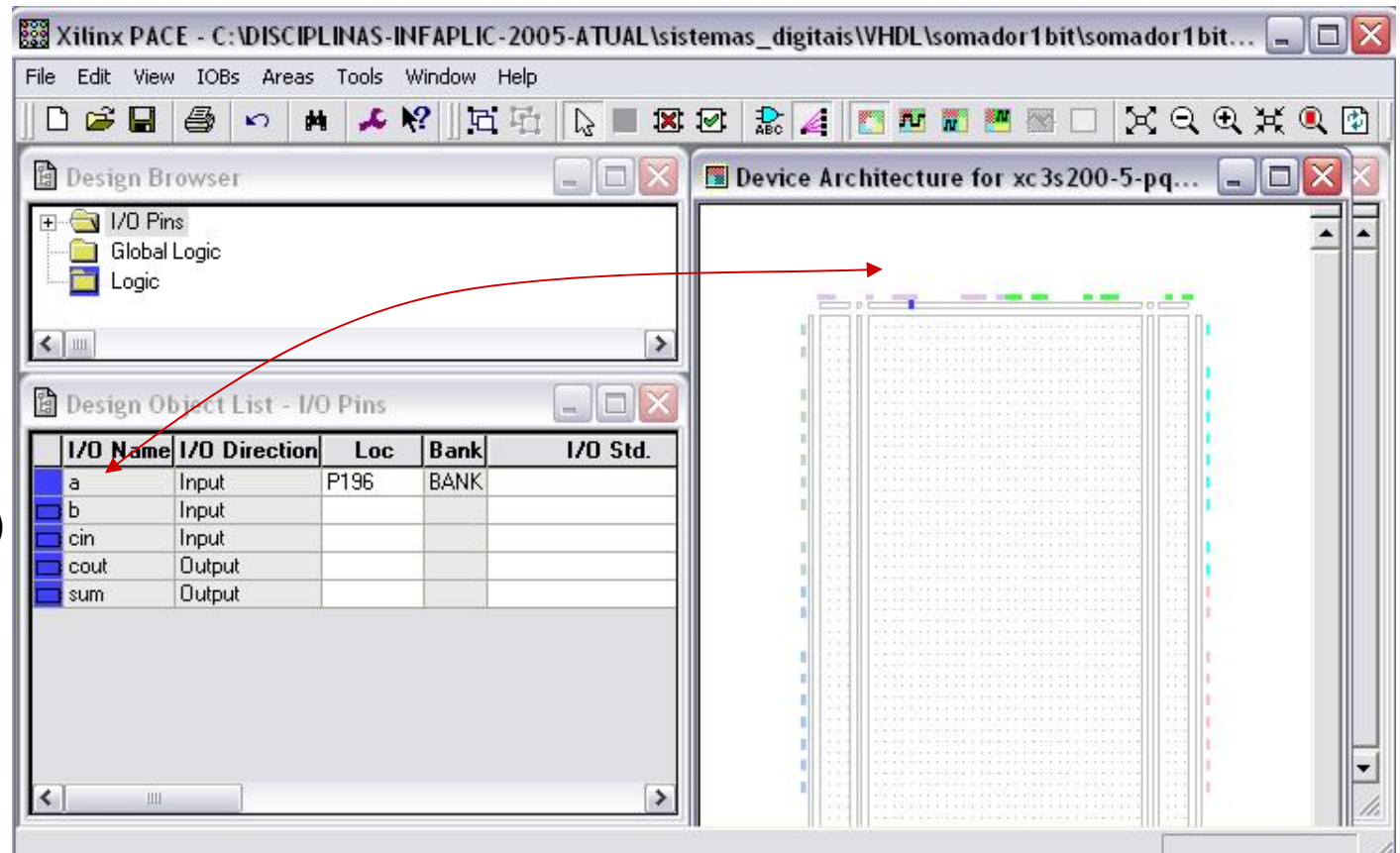


# Definindo os atributos



Conexão:

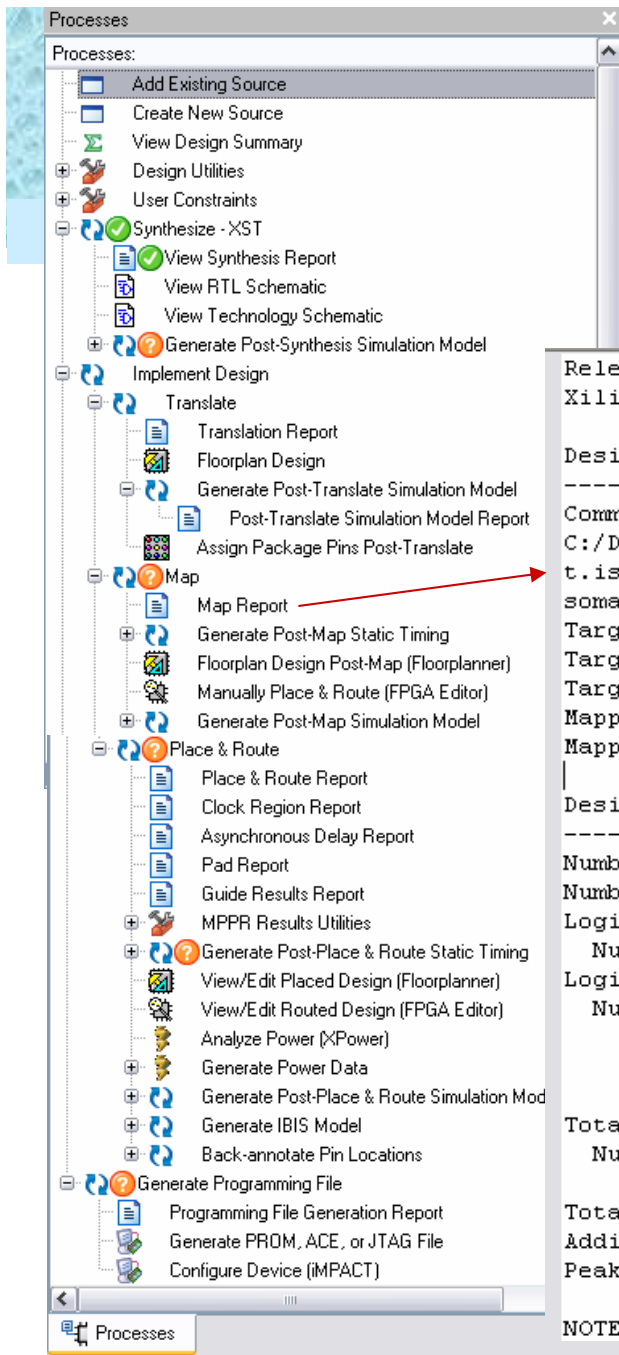
- Arrastar do mouse
- digitando o pino (pxx)



**Importante: definir os constraints (.ucf file) após ter realizado a primeira síntese.**

The screenshot shows the Xilinx ISE interface during the implementation phase. The left-hand 'Processes' pane is expanded to the 'Map' step. The main workspace displays a logic schematic titled 'Esquemático após o mapeamento', which shows the mapped logic for a 1-bit adder. The schematic includes four logic cells: two labeled 'XOR2', and two labeled 'AND2'. The inputs are 'a', 'b', and 'cin', and the outputs are 'sum' and 'cout'. The bottom pane, 'Design Objects of somador1bit', provides a summary of the mapped components:

Design Objects of somador1bit			Properties No object is selected	
Instances	Pins	Signals	Name	Value
-XLXI_1	a	a		
-XLXI_2	b	b		
-XLXI_3	cin	cin		
-XLXI_4	cout	cout		



```

Release 8.1.03i Map I.27
Xilinx Mapping Report File for Design 'somador1bit'

Design Information
-----
Command Line   : C:\Xilinx\bin\nt\map.exe -ise
                 C:/DISCIPLINAS-INFAPLIC-2005-ATUAL/sistemas_digitais/VHDL/somador1bit/somador1bi
                 t.ise -intstyle ise -p xc3s200-pq208-5 -cm area -pr b -k 4 -c 100 -o
                 somador1bit_map.ncd somador1bit.ngd somador1bit.pcf
Target Device  : xc3s200
Target Package : pq208
Target Speed   : -5
Mapper Version : spartan3 -- $Revision: 1.34 $
Mapped Date    : Sun Aug 06 11:59:30 2006

Design Summary
-----
Number of errors:      0
Number of warnings:   0
Logic Utilization:
  Number of 4 input LUTs:          2 out of  3,840   1%
Logic Distribution:
  Number of occupied Slices:              1 out of  1,920   1%
    Number of Slices containing only related logic:      1 out of    1 100%
    Number of Slices containing unrelated logic:          0 out of    1   0%
    *See NOTES below for an explanation of the effects of unrelated logic
Total Number of 4 input LUTs:          2 out of  3,840   1%
Number of bonded IOBs:                 5 out of   141   3%

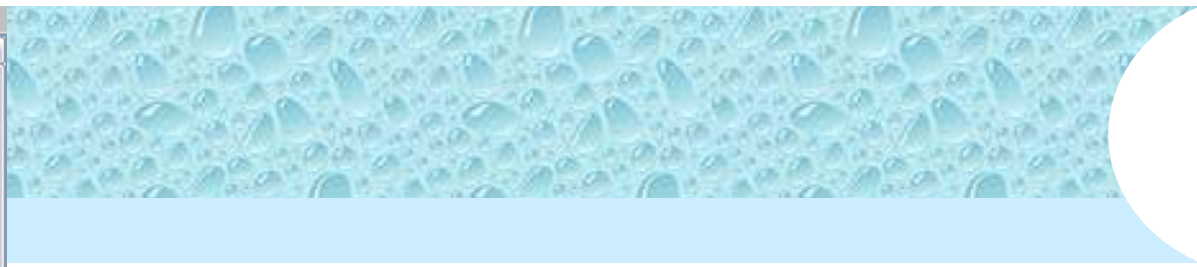
Total equivalent gate count for design: 12
Additional JT&G gate count for IOBs: 240
Peak Memory Usage: 128 MB

NOTES:

```

Processes

- Processes:
  - Add Existing Source
  - Create New Source
  - View Design Summary
  - Design Utilities
  - User Constraints
  - Synthesize - XST
    - View Synthesis Report
    - View RTL Schematic
    - View Technology Schematic
  - Generate Post-Synthesis Simulation Model
  - Implement Design
    - Translate
      - Translation Report
      - Floorplan Design
      - Generate Post-Translate Simulation Model
      - Post-Translate Simulation Model Report
      - Assign Package Pins Post-Translate
    - Map
      - Map Report
      - Generate Post-Map Static Timing
      - Floorplan Design Post-Map (Floorplanner)
      - Manually Place & Route (FPGA Editor)
      - Generate Post-Map Simulation Model
    - Place & Route
      - Place & Route Report
      - Clock Region Report
      - Asynchronous Delay Report
      - Pad Report
      - Guide Results Report
      - MPPR Results Utilities
      - Generate Post-Place & Route Static Timing
      - View/Edit Placed Design (Floorplanner)
      - View/Edit Routed Design (FPGA Editor)
      - Analyze Power (XPower)
      - Generate Power Data
      - Generate Post-Place & Route Simulation Model
      - Generate IBIS Model
      - Back-annotate Pin Locations
    - Generate Programming File
      - Programming File Generation Report
      - Generate PROM, ACE, or JTAG File
      - Configure Device (IMPACT)



Xilinx FPGA Editor - somador1bit\_map.ncd

File Edit View Tools Window Help

Array1

List1

	Name	Site	Type	#Pins	Hilite
1	a	P196	IOB	1	no cd
2	b		IOB	1	no cd
3	cin		IOB	1	no cd
4	cout		IOB	1	no cd
5	cout_		SLICE	8	no cd
6	sum		IOB	1	no cd

World1

layer buttons, and then clicking on the apply button again.

For Help, press F1

xc3s200-5pq208 No Logic Changes

# Programando na placa

Processes:

- Add Existing Source
- Create New Source
- View Design Summary
- Design Utilities
- User Constraints
- Synthesize - XST
- Implement Design
  - Translate
  - Map
    - Map Report
    - Generate Post-Map Static Timing
    - Floorplan Design Post-Map (Floorplanner)
    - Manually Place & Route (FPGA Editor)
    - Generate Post-Map Simulation Model
  - Place & Route
  - Generate Programming File
    - Programming File Generation Report
    - Generate PROM, ACE, or JTAG File
    - Configure Device (iMPACT)

iMPACT - C:/DISCIPLINAS-INFAPLIC-2005-ATUAL/sistemas\_digitais/VHDL/somador1bit/somador1bit.ipf

File Edit View Operations Options Output Debug Window Help

Flows

- Boundary Scan
- SlaveSerial
- SelectMAP
- Desktop Configur...
- SystemACE

iMPACT Modes

iMPACT Processes

iMPACT Process Operations

Welcome to iMPACT

Transcript

Output Error Warning

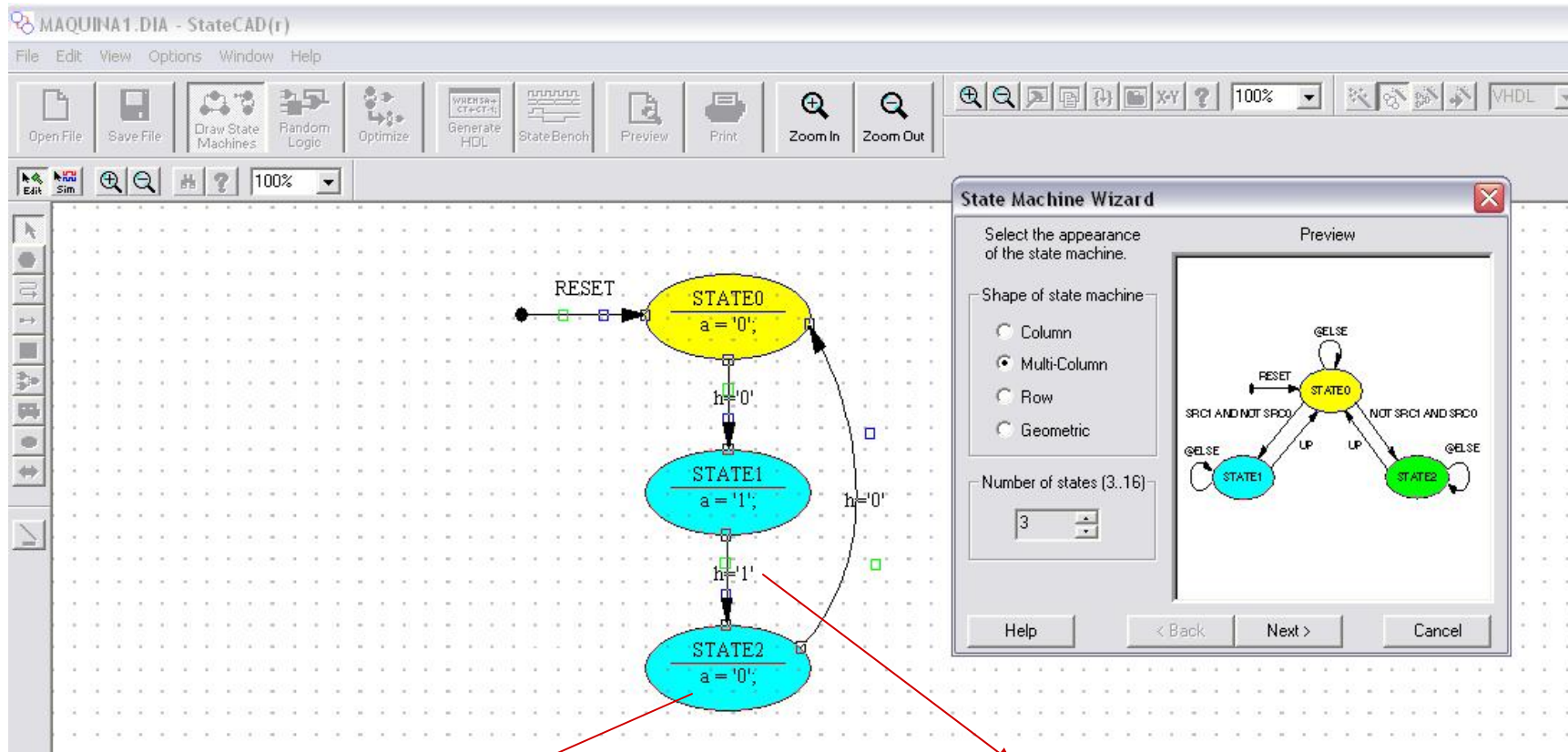
IMPACT - Welcome to iMPACT

Please select an action from the list below

- Configure devices using Boundary-Scan (JTAG)
  - Automatically connect to a cable and identify Boundary-Scan chain
- Prepare a PROM File
- Prepare a System ACE File
- Prepare a Boundary-Scan File
- Configure devices
  - SVF
  - using Slave Serial mode

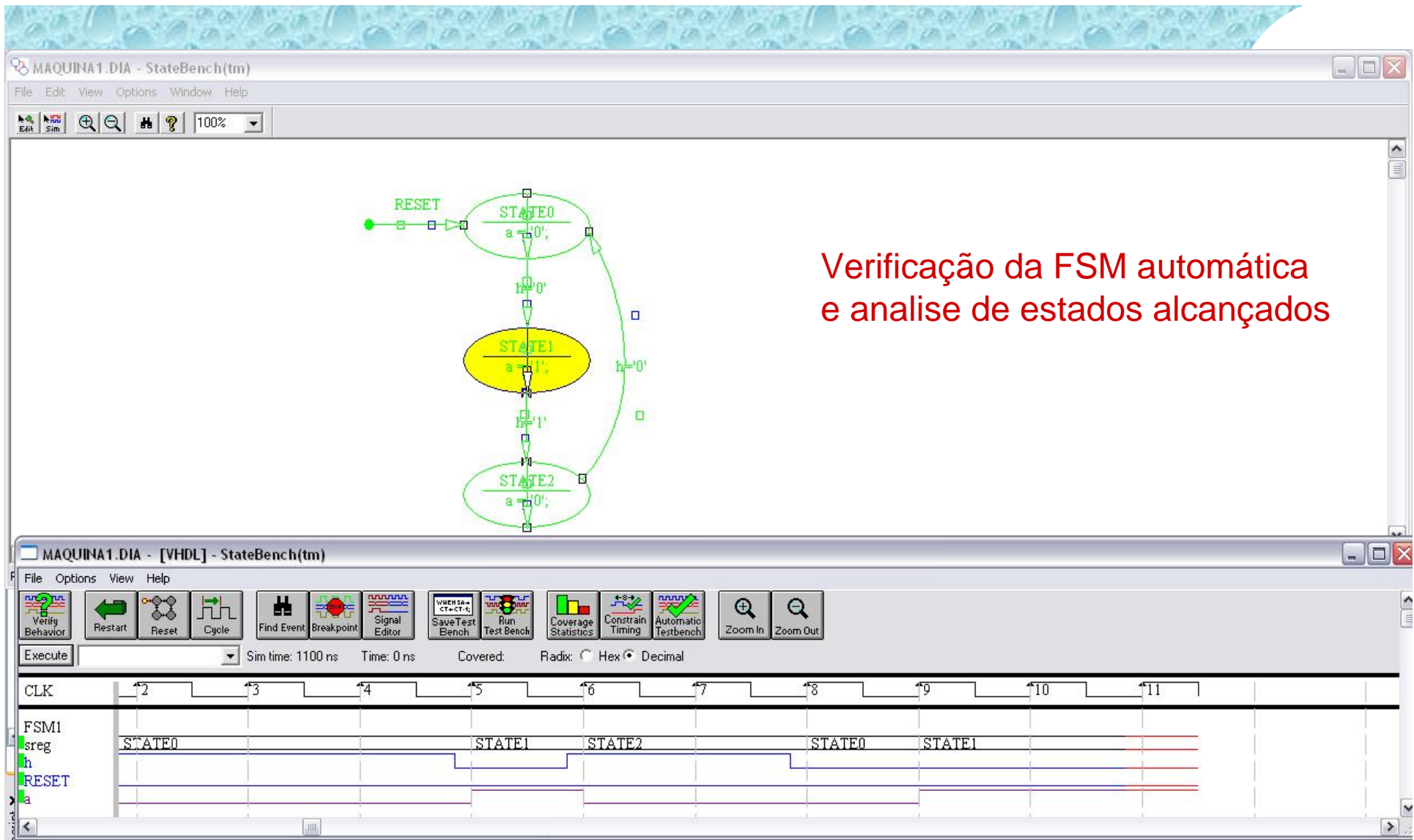
< Back Finish Cancel

# Entrada como Diagrama de Estados



Saida  
nome = 'valor'; ou nome = "valor";

Condição  
entrada = 'valor' ou entrada = "valor"  
(sem ;)



Verificação da FSM automática e análise de estados alcançados

The screenshot shows the Xilinx ISE interface. The top window title is "Xilinx - ISE - C:\DISCIPLINAS-INFAPLIC-2005-ATUAL\istemas\_digitais\WHDL\somador1bit\somador1bit.ise - [somador1bit.sch]". The menu bar includes File, Edit, View, Project, Source, Process, Add, Tools, Window, and Help. The toolbar contains various icons for file operations and design tools. The "Sources" pane on the left shows a tree view for "Sources for Synthesis/Implementation" with files: somador1bit, xc3s200-5pq208, and somador1bit (somador1bit.sch). The "Processes" pane in the center lists: Add Existing Source, Create New Source, View Design Summary, Design Utilities, User Constraints, Synthesize - XST, Implement Design, and Generate Programming File. The main workspace displays a logic diagram of a 1-bit adder with two 4-bit inputs (a and b), two 4-bit outputs (sum and cin), and an AND gate. The "Generate Programming File" process is highlighted in the "Processes" pane. The "Transcript" window at the bottom shows the message: "Started : 'Generate Programming File'." and "Process 'Generate Programming File' completed successfully". The status bar at the bottom left says "Ready" and the bottom right shows the device ID "T2552.5001".

Escolher entre síntese e simulação no ISE  
(importante: arquivos de testbench só aparecerão no modo simulação).

# Simulando no ISE