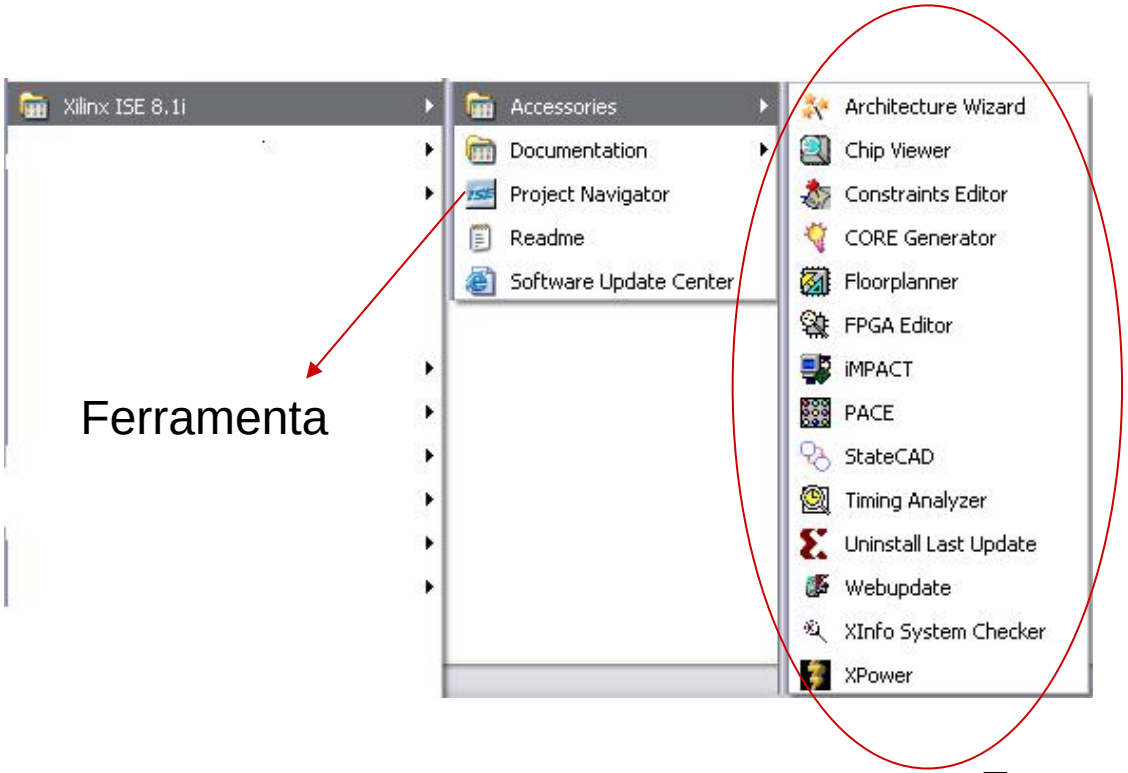
Tutorial ISE

- Descrição esquemático
- Descrição Maquina de Estados
- Síntese
- Simulação

UFRGS

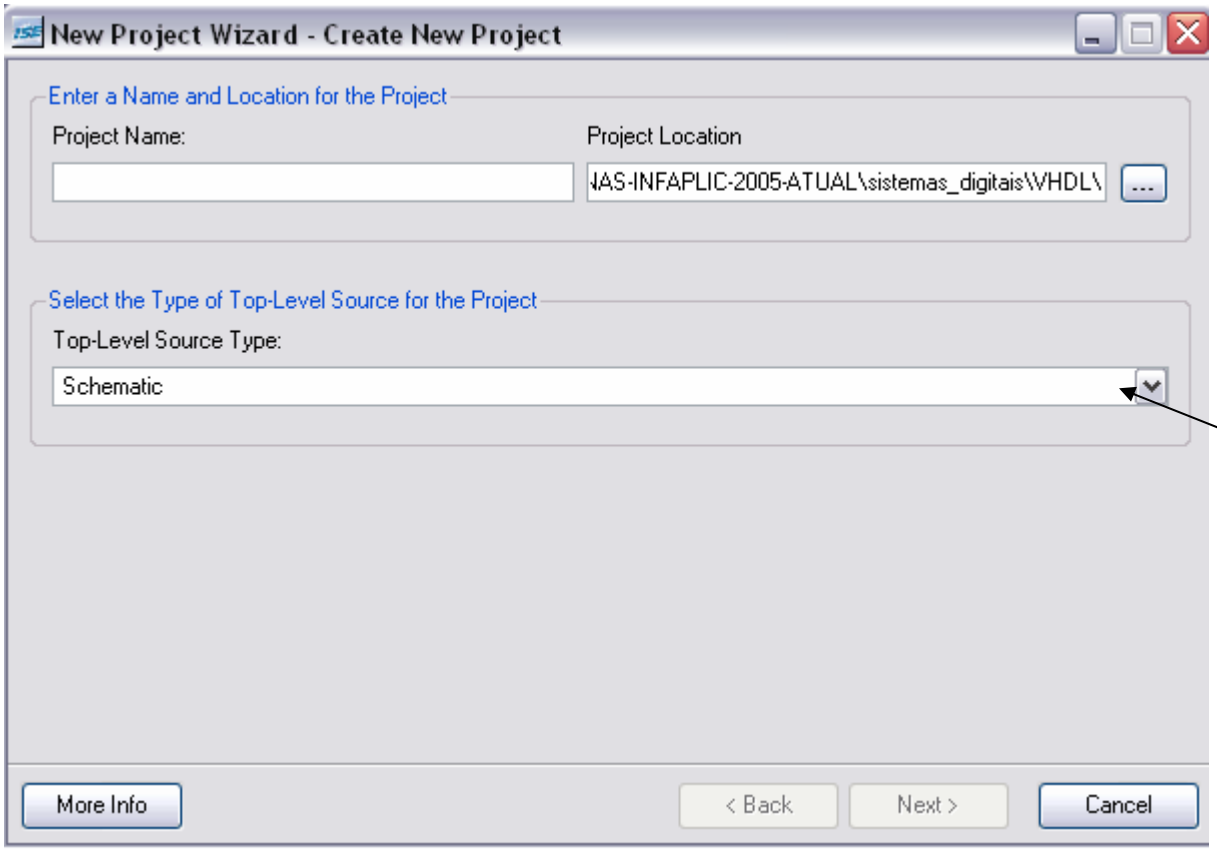
ISE

- **www.xilinx.com** (documentação)



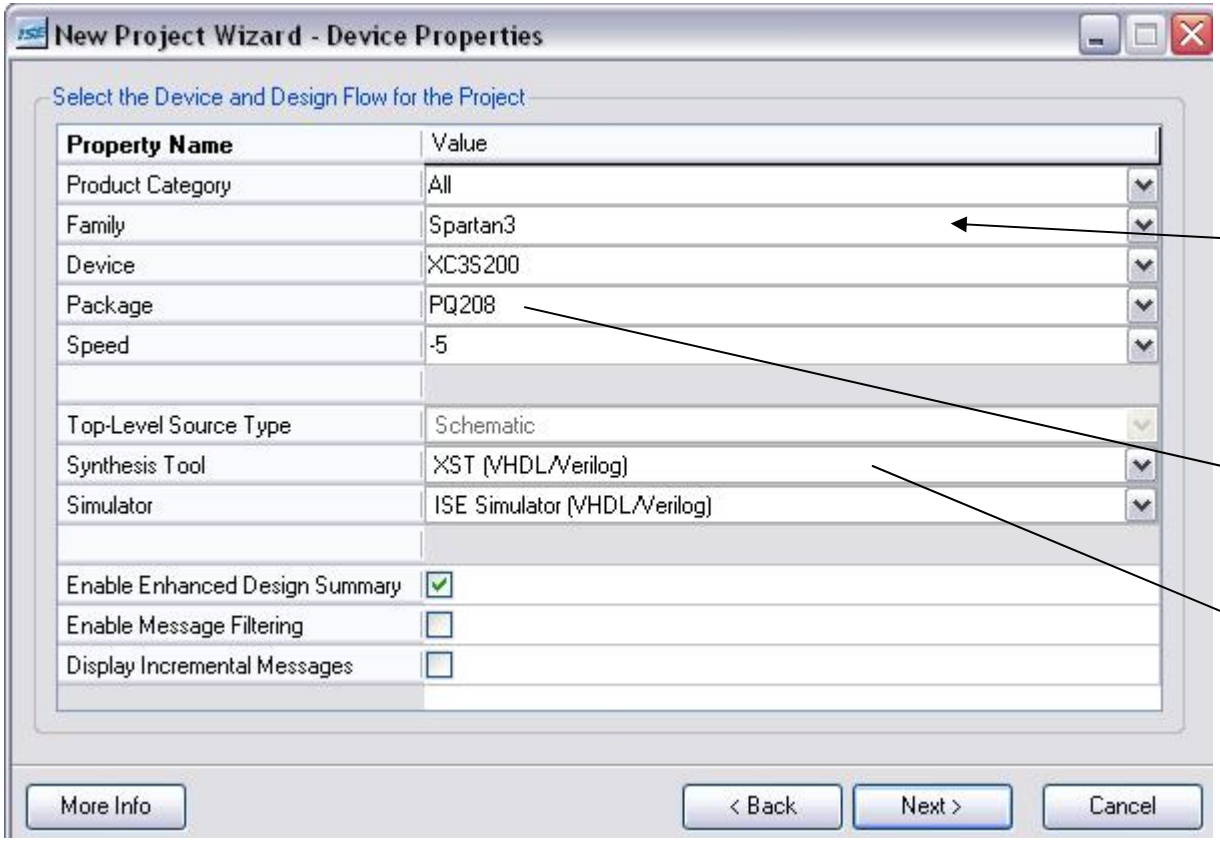
Ferramentas auxiliares que podem ser chamadas de dentro do Project Navigator

Passo 1: Criar um novo projeto



Escolher entre:
- Esquemático
- HDL

Passo 2: Escolhar FPGA e ferramentas

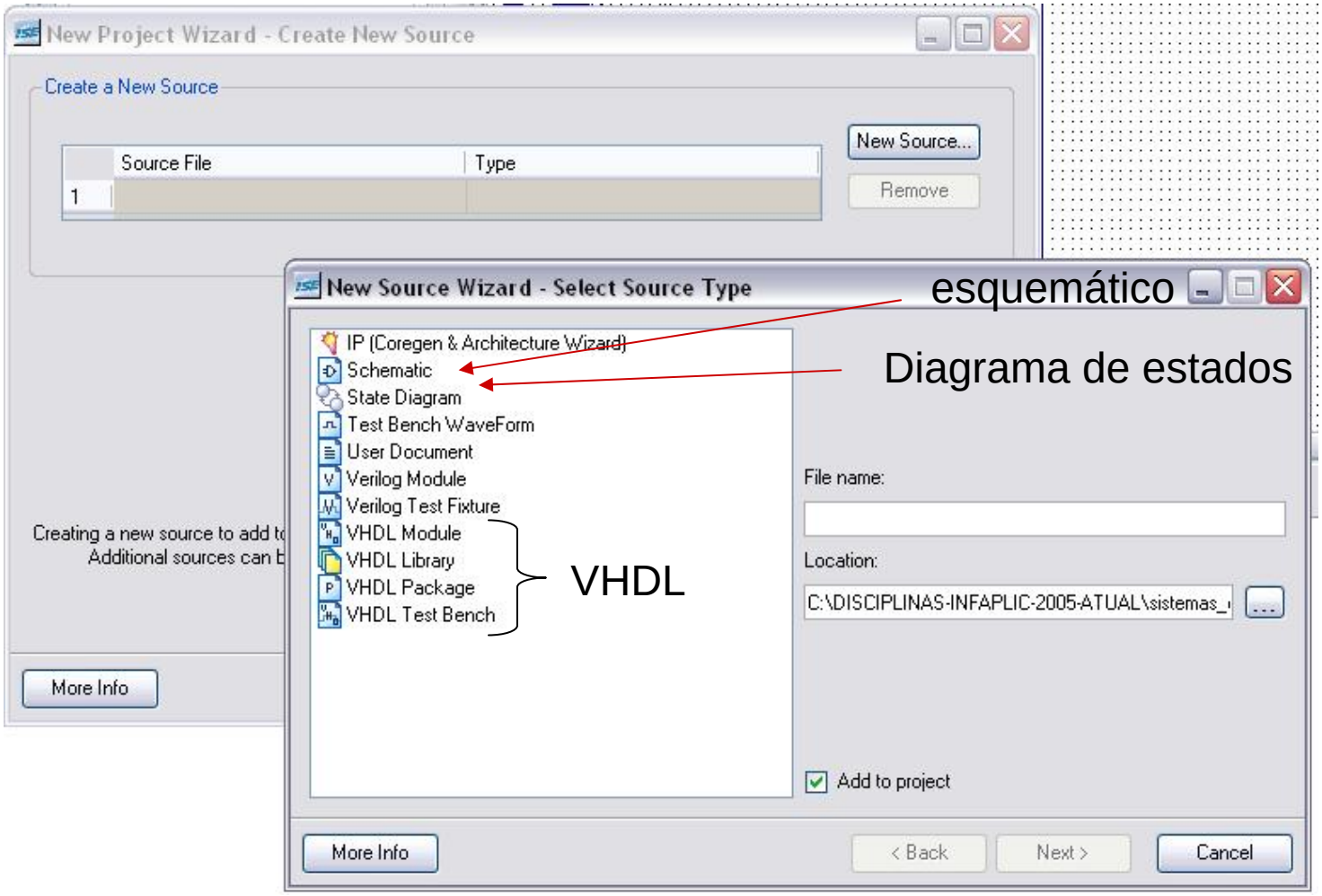


Escolher a familia e o FPGA

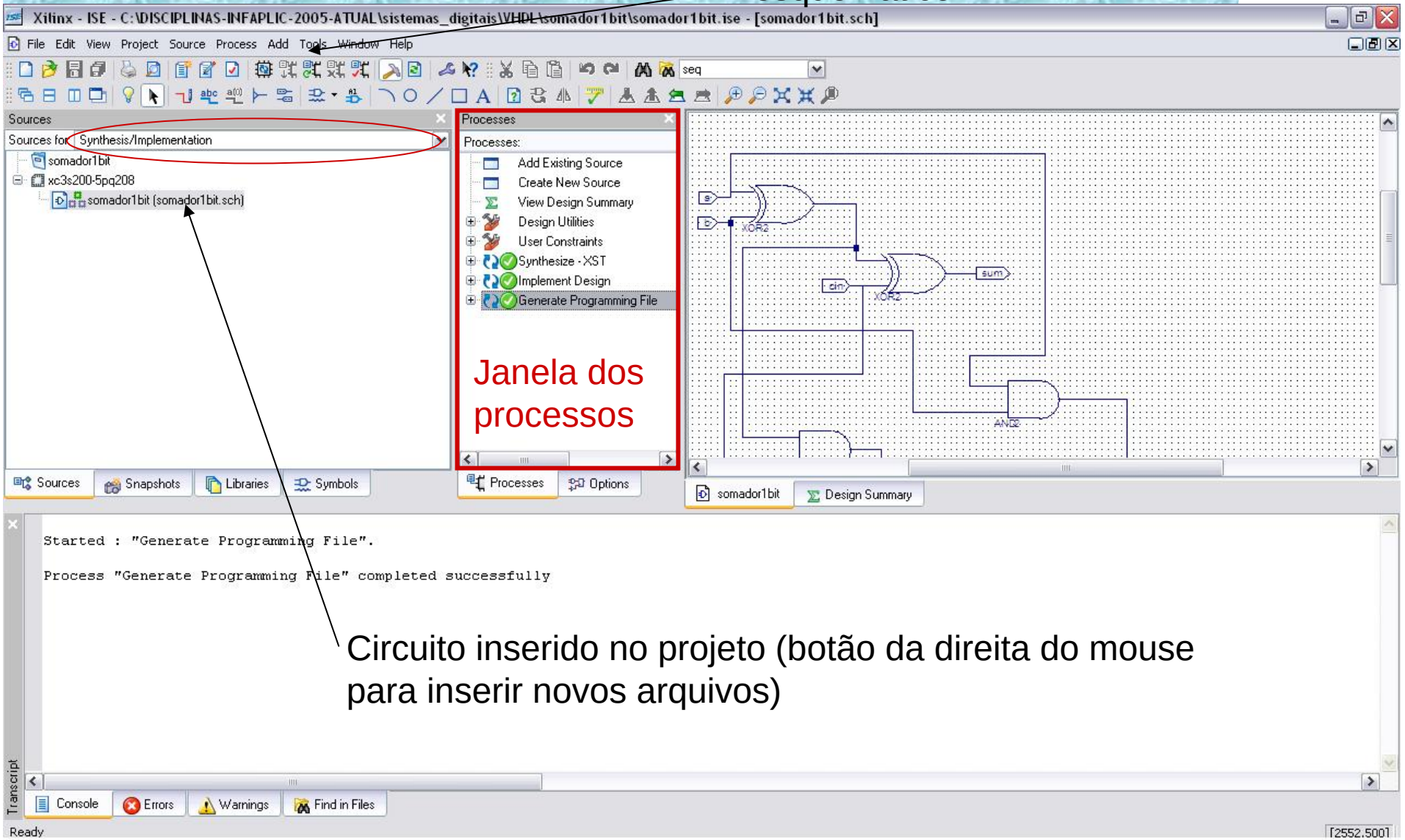
encapsulamento

Ferramentas de síntese e o simulador

Passo 3: Criar um novo circuito (fonte)

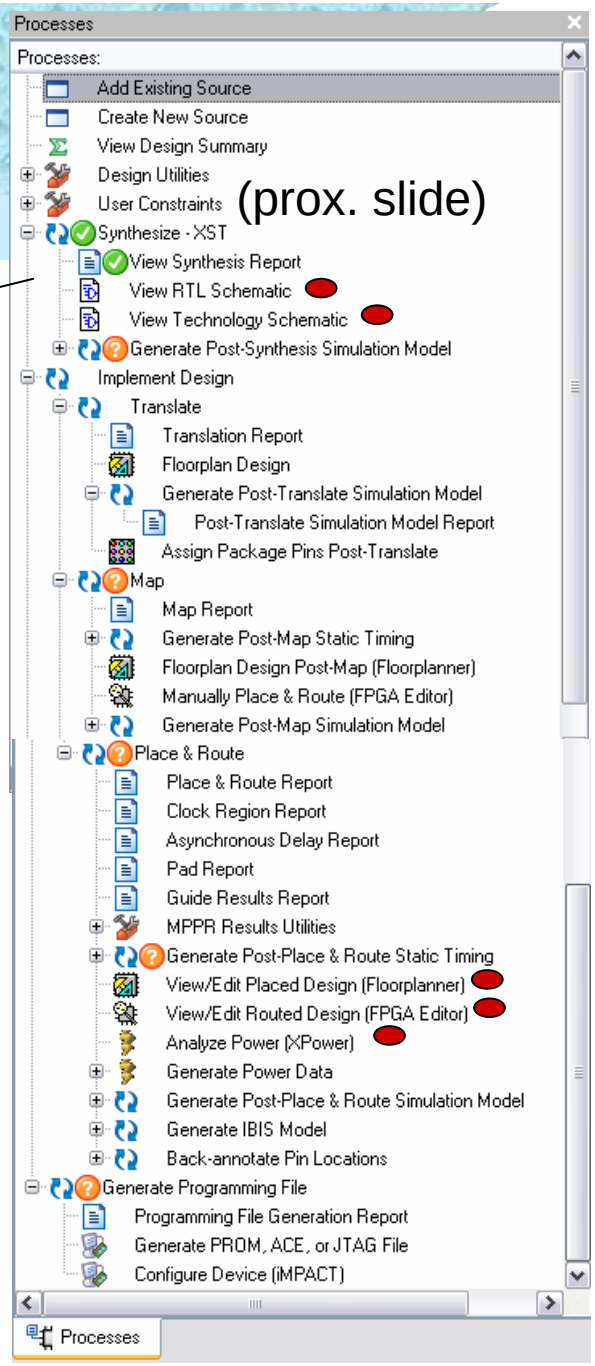


Inserir instancias e portas no esquemático



Circuito inserido no projeto (botão da direita do mouse para inserir novos arquivos)

Analisando os processos



(prox. slide)

Sintese inicial (mapeamento para biblioteca padrão de nands e nors)

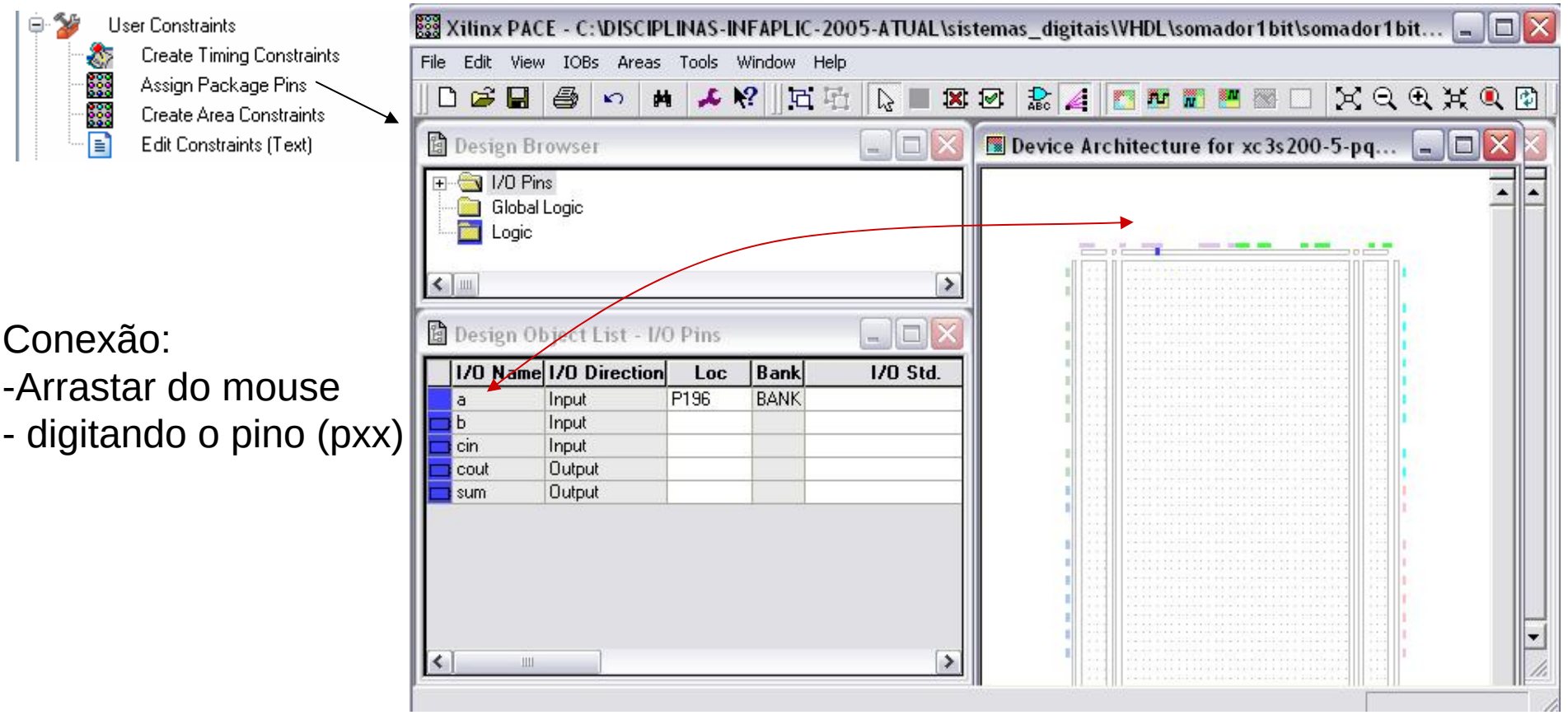
Todo o processo tem propriedades que podem ser configuradas
(basta apertar o botão da direita do mouse em cima do processo).

Para rodar um processo basta apertar RUN (usando o botão da direita do mouse ou double click)

- Todas estes processos ao fazer um “double click” uma nova janela irá abrir mostrando o resultado ou nova ferramenta.

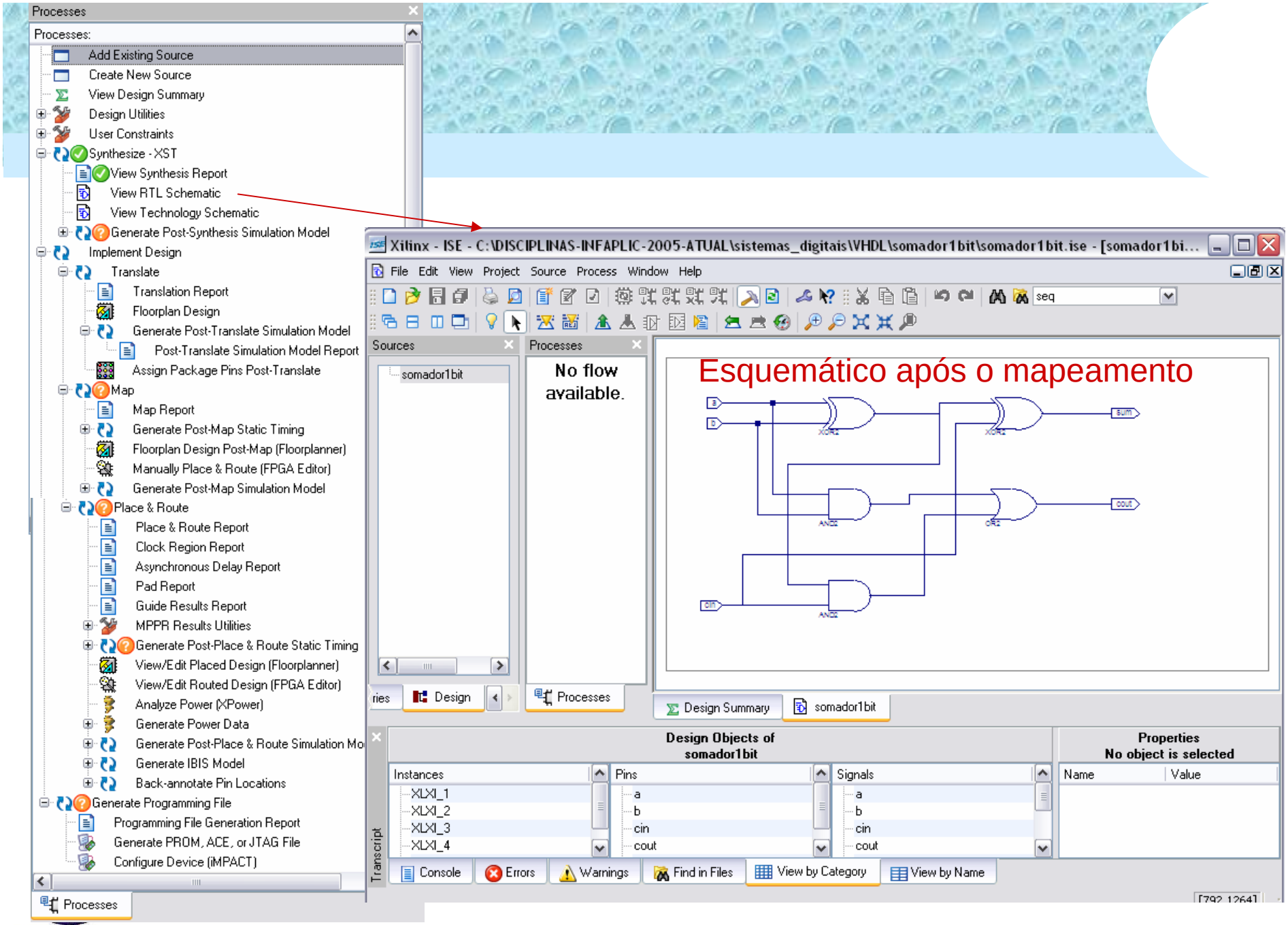
UFRGS

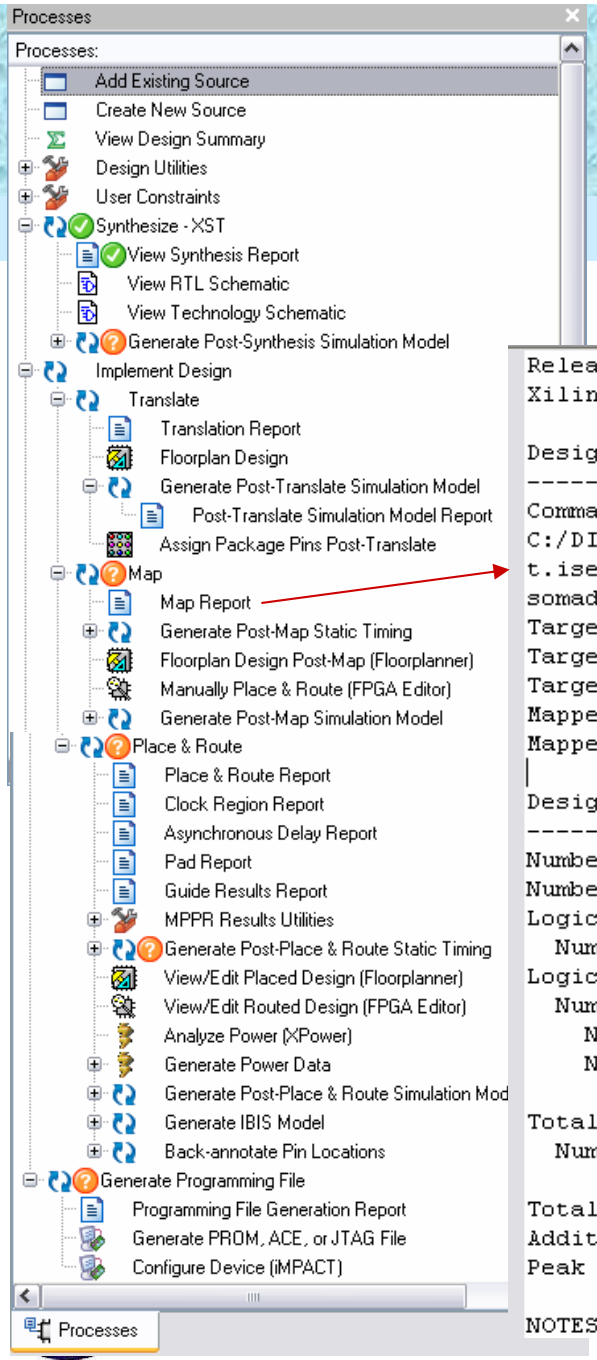
Definindo os atributos



Conexão:
-Arrastar do mouse
- digitando o pino (pxx)

Importante: definir os constraints (.ucf file) após ter realizado a primeira sintese.


Processes
Processes:
Add Existing Source
Create New Source
View Design Summary
Design Utilities
User Constraints
Synthesize - XST
View Synthesis Report
View RTL Schematic
View Technology Schematic
Generate Post-Synthesis Simulation Model
Implement Design
Translate
Translation Report
Floorplan Design
Generate Post-Translate Simulation Model
Post-Translate Simulation Model Report
Assign Package Pins Post-Translate
Map
Map Report
Generate Post-Map Static Timing
Floorplan Design Post-Map (Floorplanner)
Manually Place & Route (FPGA Editor)
Generate Post-Map Simulation Model
Place & Route
Place & Route Report
Clock Region Report
Asynchronous Delay Report
Pad Report
Guide Results Report
MPPR Results Utilities
Generate Post-Place & Route Static Timing
View/Edit Placed Design (Floorplanner)
View/Edit Routed Design (FPGA Editor)
Analyze Power (XPower)
Generate Power Data
Generate Post-Place & Route Simulation Mo
Generate IBIS Model
Back-annotate Pin Locations
Generate Programming File
Programming File Generation Report
Generate PROM, ACE, or JTAG File
Configure Device (iMPACT)
Processes
Xilinx - ISE - C:\DISCIPLINAS-INFAPLIC-2005-ATUAL\sistemas_digitais\VHDL\somador1bit\somador1bit.ise - [somador1bi...
File Edit View Project Source Process Window Help
seq
Sources
somador1bit
Processes
No flow available.
Esquemático após o mapeamento
Design
Processes
Design Summary
somador1bit
Design Objects of somador1bit
Instances
XLXI_1
XLXI_2
XLXI_3
XLXI_4
Pins
a
b
cin
cout
Signals
a
b
cin
cout
Properties
No object is selected
Name
Value
Transcript
Console
Errors
Warnings
Find in Files
View by Category
View by Name



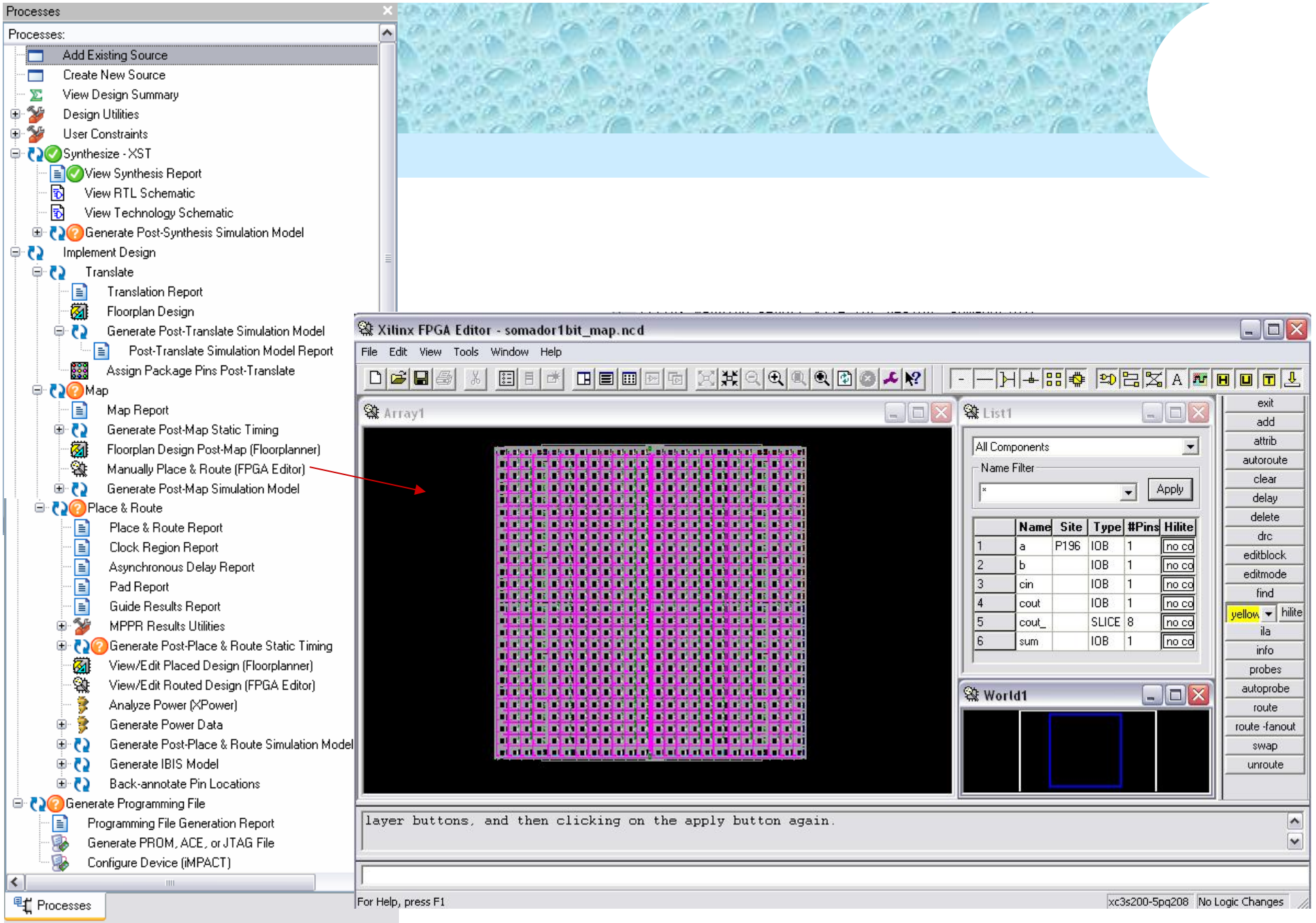

```
Release 8.1.03i Map I.27
Xilinx Mapping Report File for Design 'somador1bit'

Design Information
------------------
Command Line   : C:\Xilinx\bin\nt\map.exe -ise
C:/DISCIPLINAS-INFAPLIC-2005-ATUAL/sistemas_digitais/VHDL/somador1bit/somador1bi
t.ise -intstyle ise -p xc3s200-pq208-5 -cm area -pr b -k 4 -c 100 -o
somador1bit_map.ncd somador1bit.ngd somador1bit.pcf
Target Device  : xc3s200
Target Package : pq208
Target Speed   : -5
Mapper Version : spartan3 -- $Revision: 1.34 $
Mapped Date    : Sun Aug 06 11:59:30 2006

Design Summary
--------------
Number of errors:      0
Number of warnings:    0
Logic Utilization:
  Number of 4 input LUTs:                2 out of   3,840    1%
Logic Distribution:
  Number of occupied Slices:                             1 out of   1,920    1%
    Number of Slices containing only related logic:      1 out of       1  100%
    Number of Slices containing unrelated logic:         0 out of       1    0%
      *See NOTES below for an explanation of the effects of unrelated logic
Total Number of 4 input LUTs:          2 out of   3,840    1%
  Number of bonded IOBs:               5 out of     141    3%

Total equivalent gate count for design:  12
Additional JTAG gate count for IOBs:  240
Peak Memory Usage:  128 MB

NOTES:
```


Processes
Processes:
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User Constraints
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View RTL Schematic
View Technology Schematic
Generate Post-Synthesis Simulation Model
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Assign Package Pins Post-Translate
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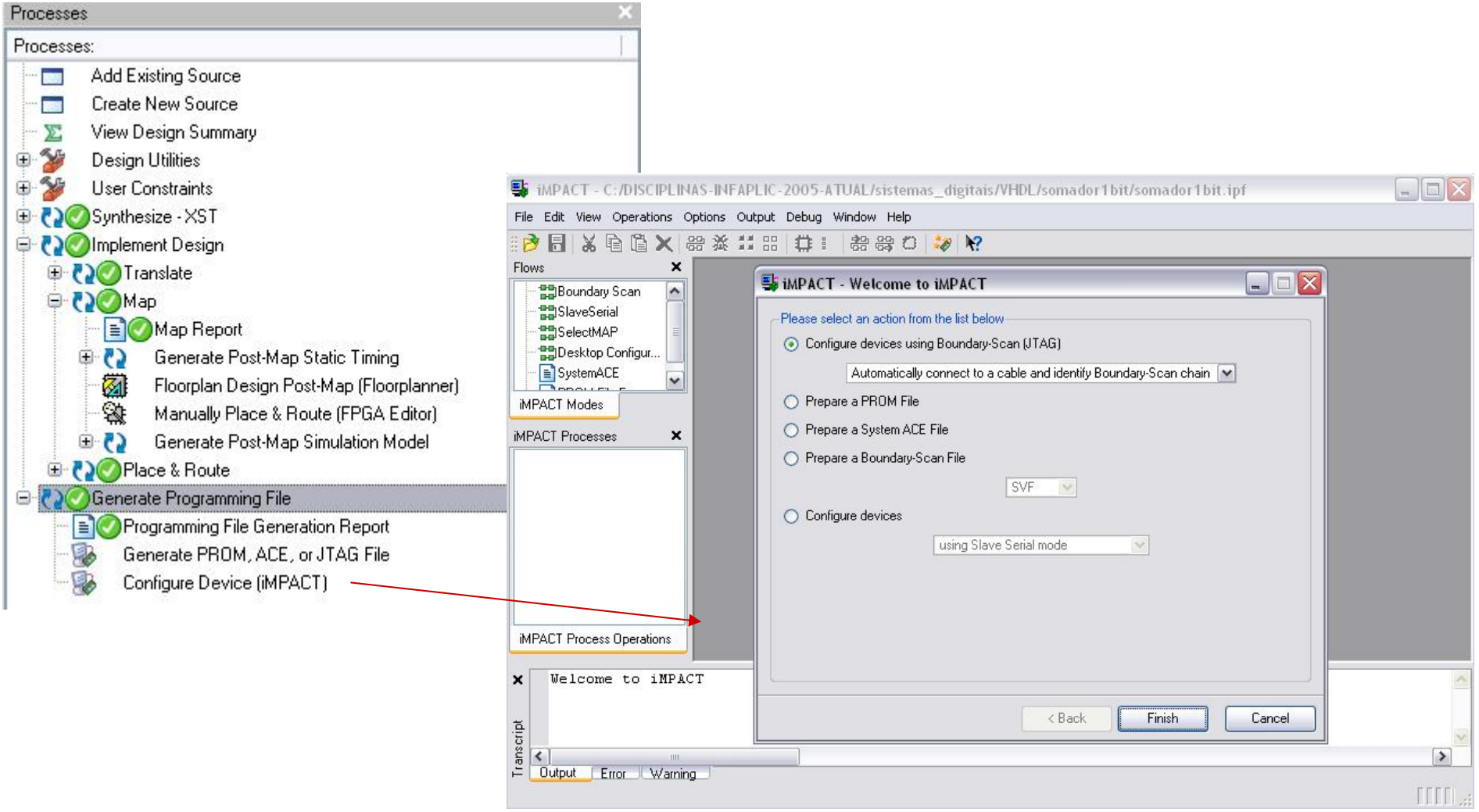
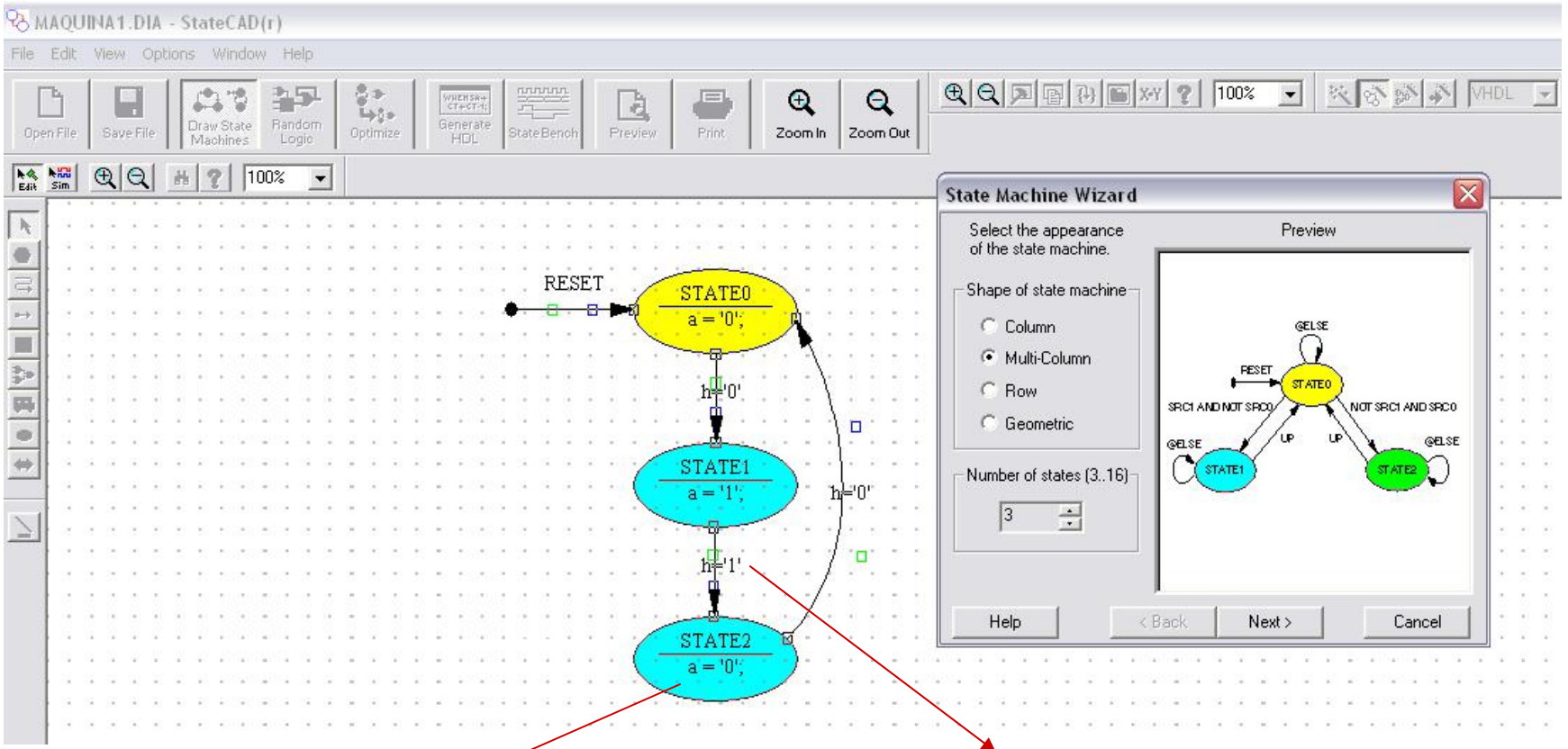
Generate Programming File
Programming File Generation Report
Generate PROM, ACE, or JTAG File
Configure Device (iMPACT)
Processes
Xilinx FPGA Editor - somador1bit_map.ncd
File Edit View Tools Window Help
Array1
List1
All Components
Name Filter
Apply
Name Site Type #Pins Hilite
1 a P196 IOB 1 no co
2 b IOB 1 no co
3 cin IOB 1 no co
4 cout IOB 1 no co
5 cout_ SLICE 8 no co
6 sum IOB 1 no co
World1
exit
add
attrib
autoroute
clear
delay
delete
drc
editblock
editmode
find
yellow
hilite
ila
info
probes
autoprobe
route
route -fanout
swap
unroute
layer buttons, and then clicking on the apply button again.
For Help, press F1
xc3s200-5pq208
No Logic Changes

Programando na placa

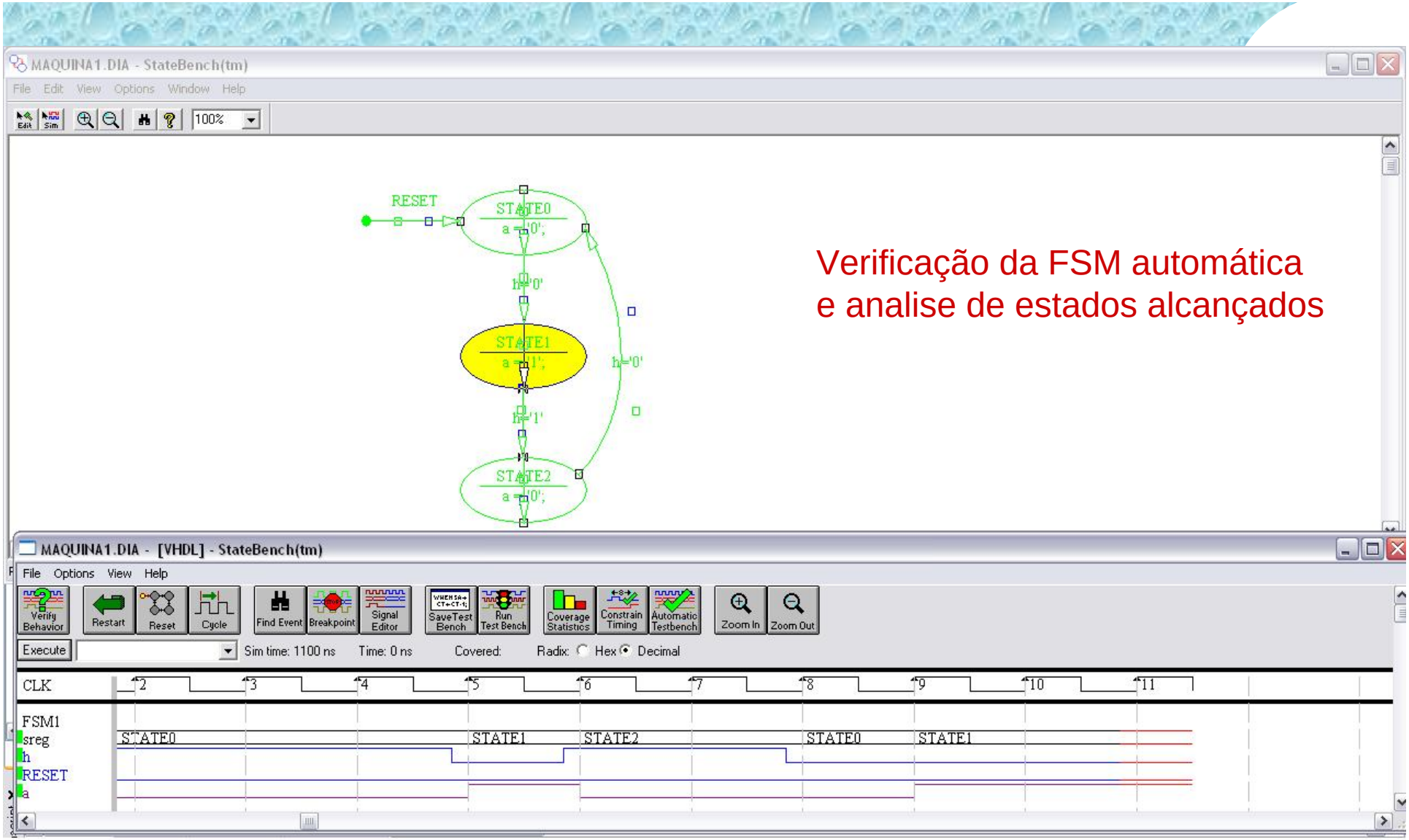


Entrada como Diagrama de Estados

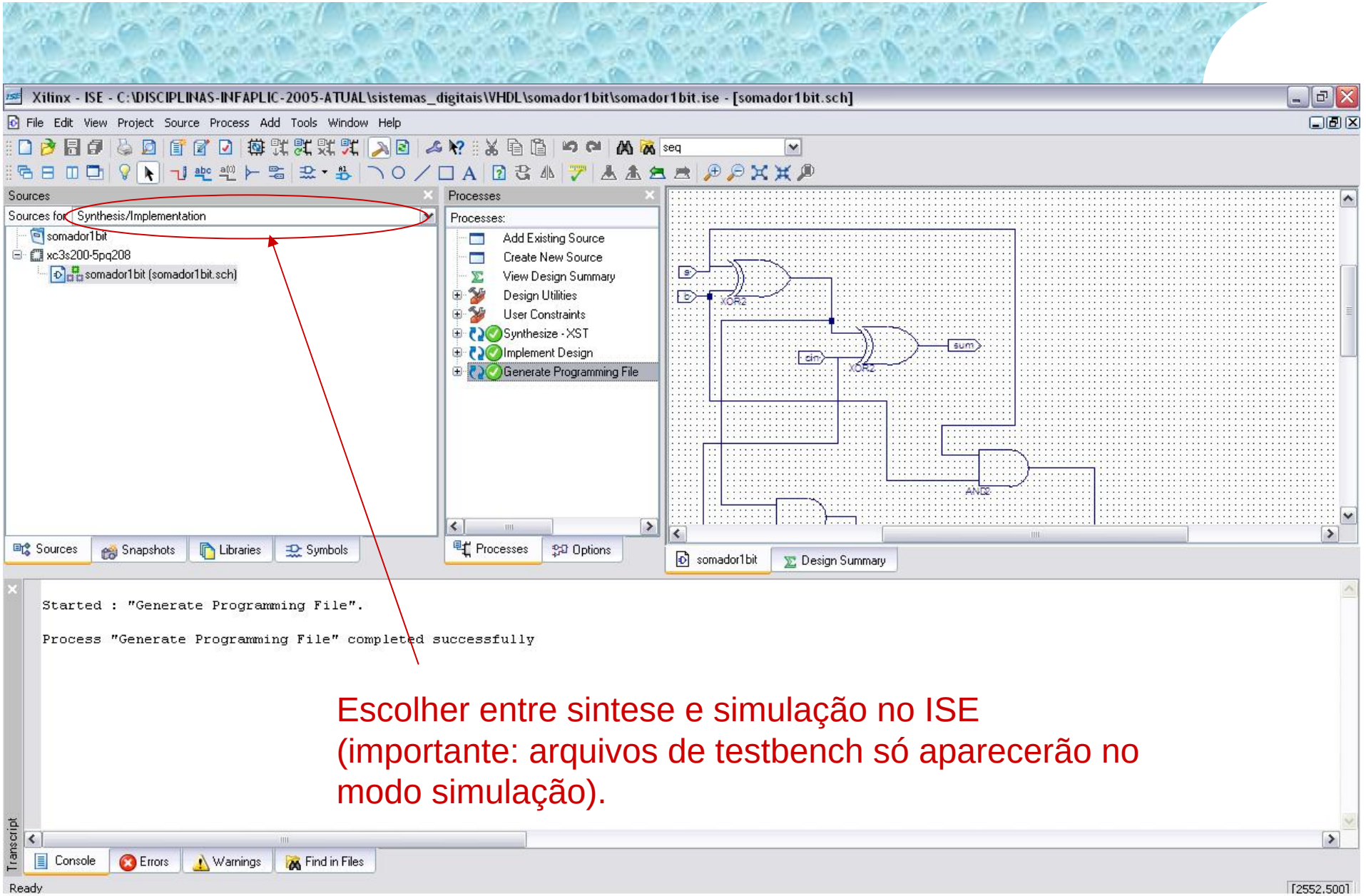


Saida
nome = ‘valor’; ou nome = “valor”;

Condição
entrada = ‘valor’ ou entrada =“valor”
(sem ;)



Verificação da FSM automática
e analise de estados alcançados



Escolher entre sintese e simulação no ISE
(importante: arquivos de testbench só aparecerão no modo simulação).

Simulando no ISE