INF01058

Circuitos Digitais

Transistor MOS
Portas CMOS

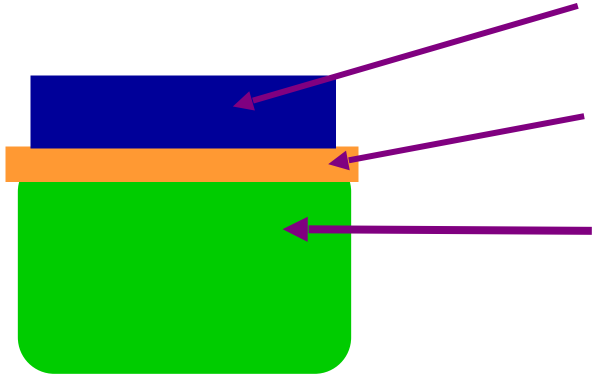
UFRGS

.inf INSTITUTO DE INFORMÁTICA UFRGS

Aula 2a

Transistor MOS

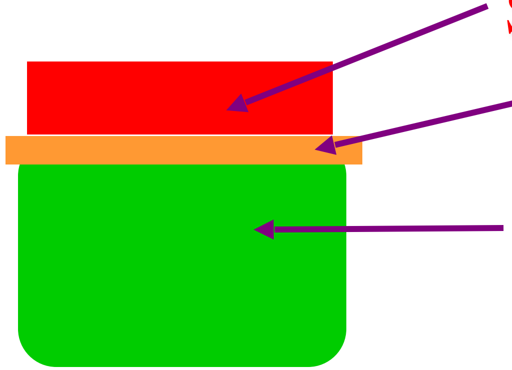
Estruturas MOS



Metal

Óxido de Silício SiO_2

Semicondutor Germânio ou
Silício Monocristalino

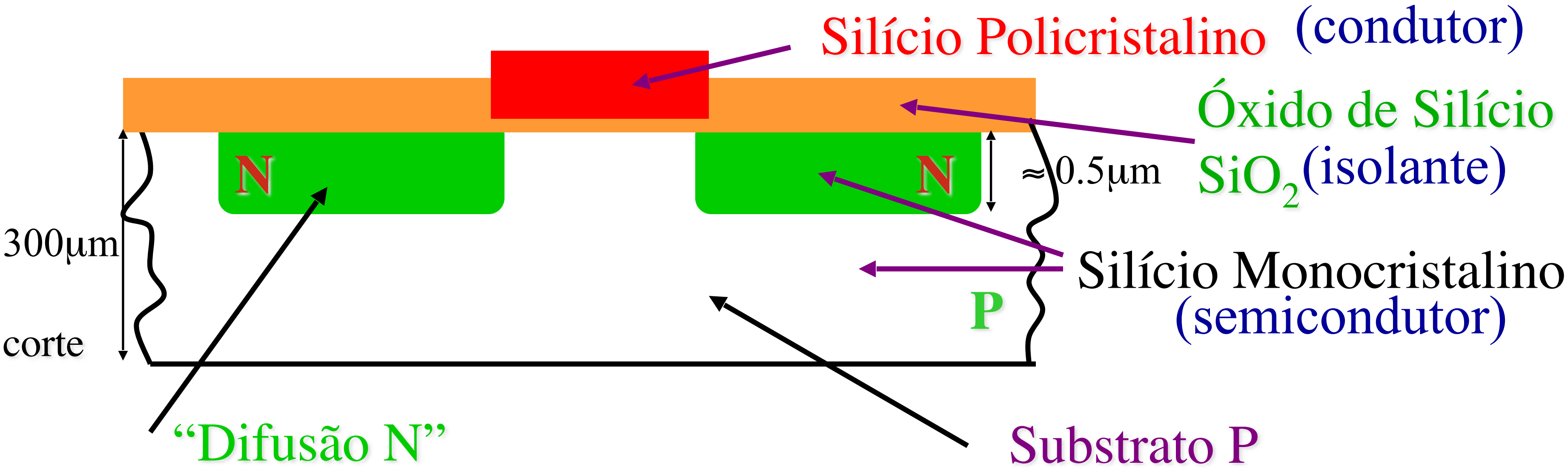


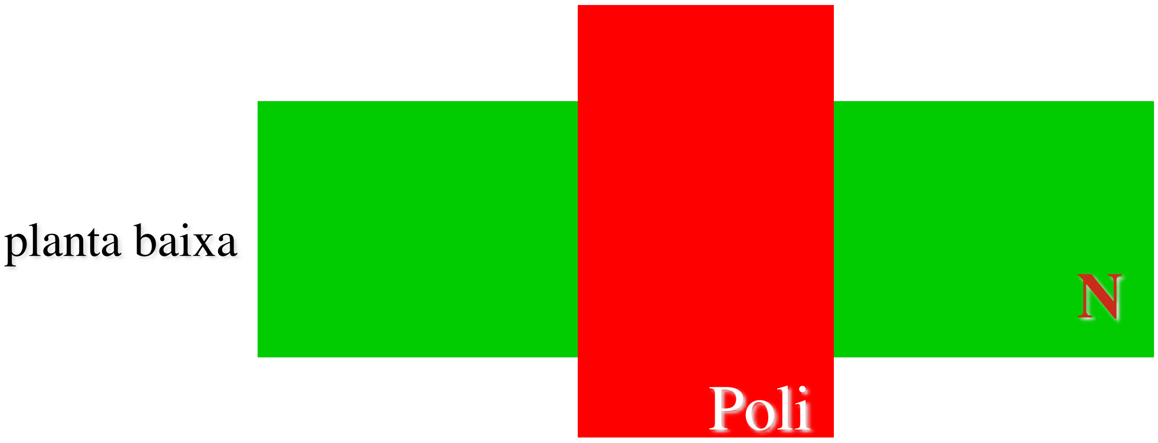
Silício Policristalino CONDUTOR

Óxido de Silício SiO_2 ISOLANTE

Silício Monocristalino SEMICONDUTOR

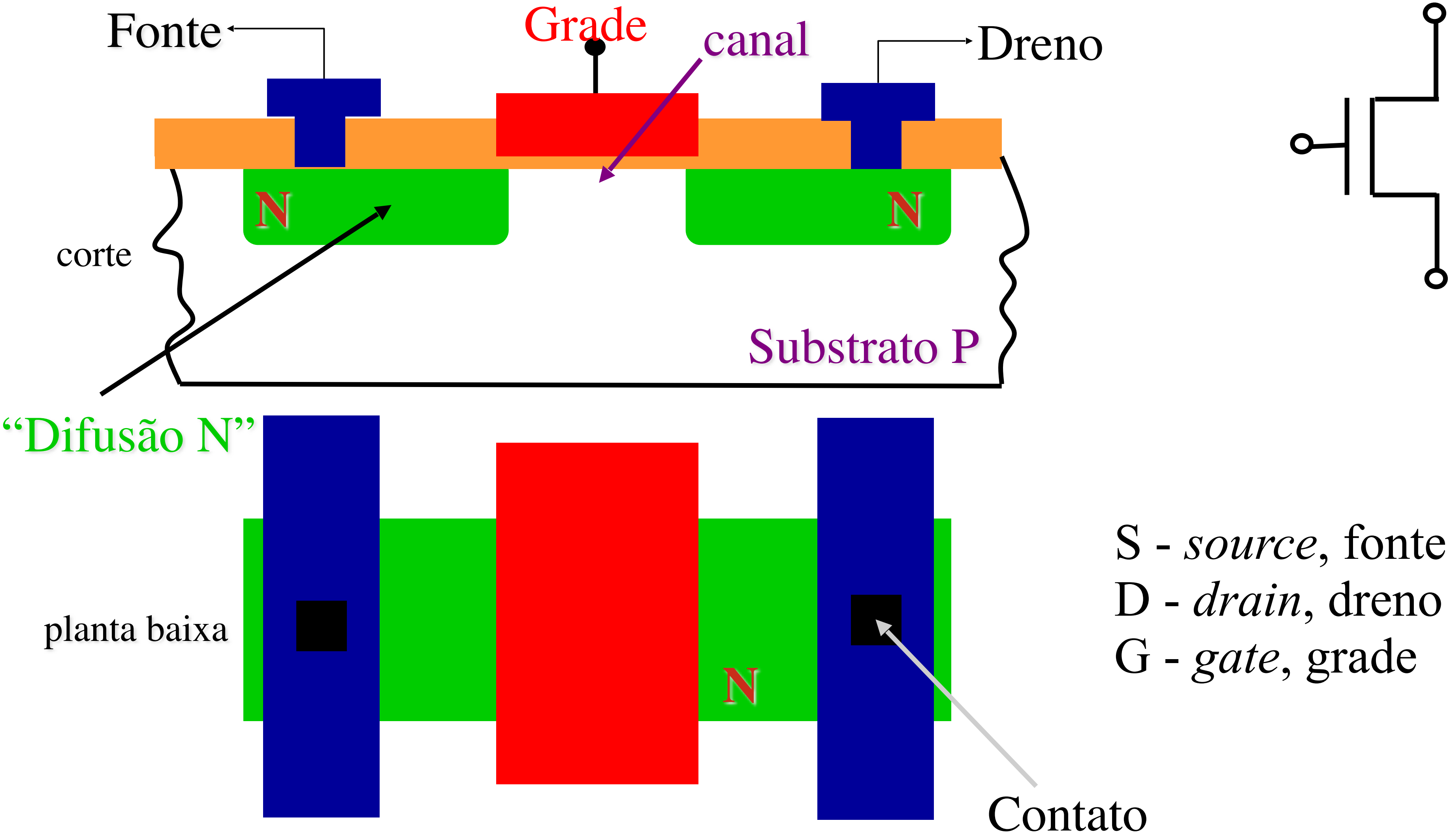
Transistor MOS


Silício Policristalino (condutor)
Óxido de Silício
SiO_2(isolante)
N
N
≈0.5μm
300μm
corte
Silício Monocristalino
(semicondutor)
P
"Difusão N"
Substrato P


planta baixa
N
Poli

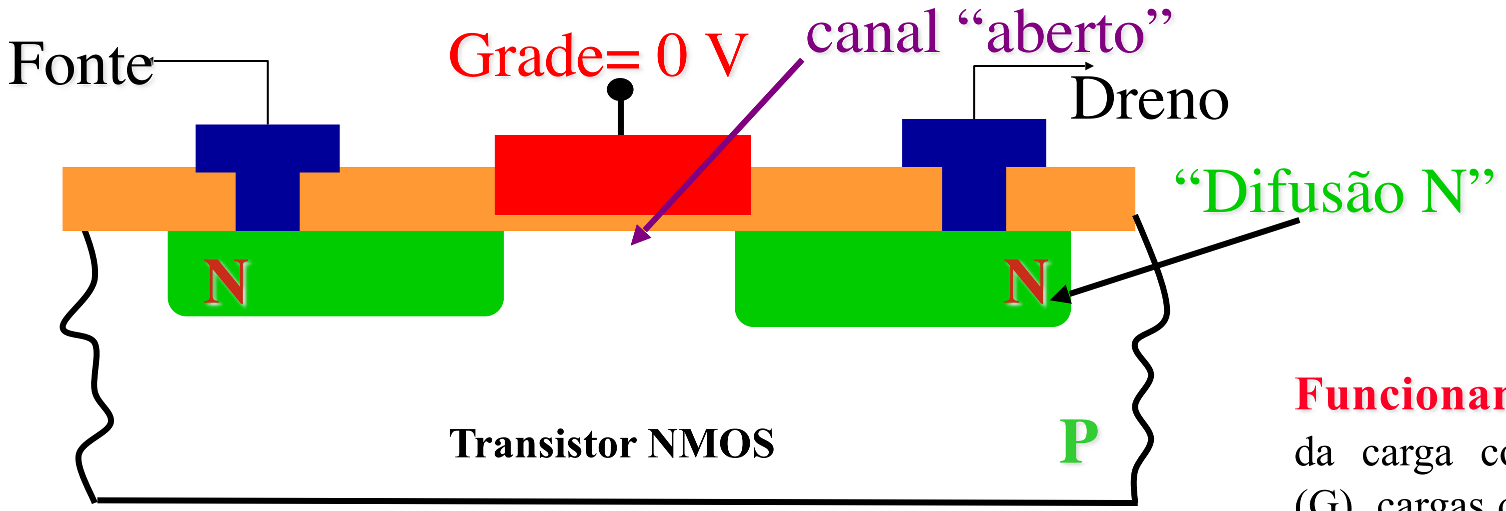
2 Tipos:
- **PMOS**
- **NMOS**

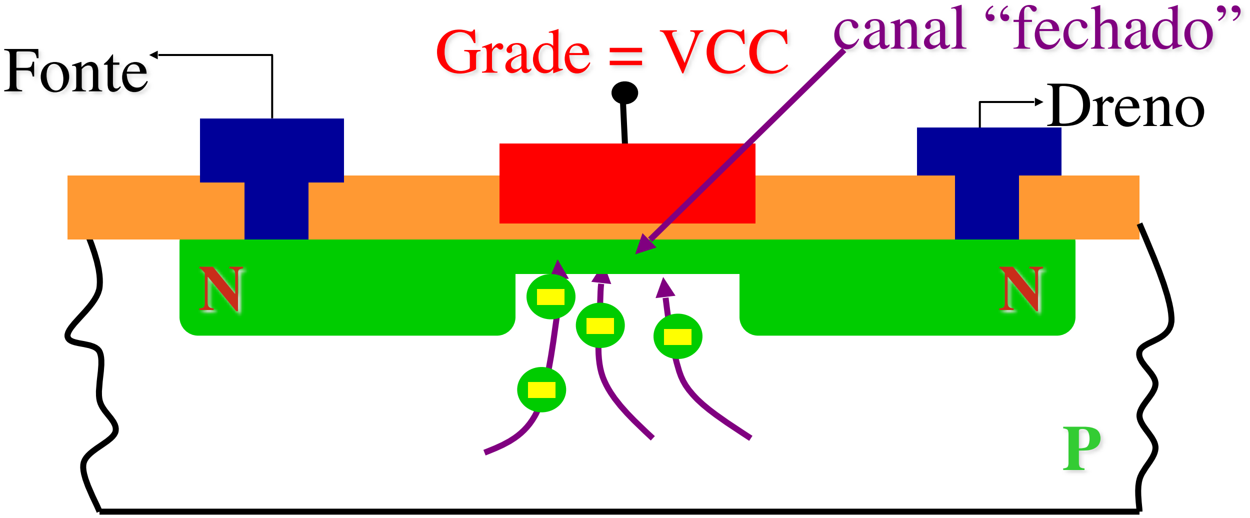
Transistor MOS

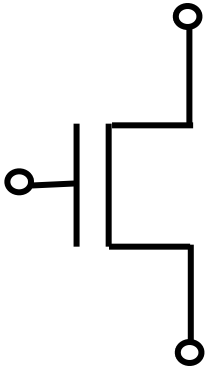

Fonte
Grade
canal
Dreno
N
N
corte
Substrato P
"Difusão N"
planta baixa
N
Contato

S - *source*, fonte
D - *drain*, dreno
G - *gate*, grade

Transistor MOS


Fonte
Grade= 0 V
canal "aberto"
Dreno
"Difusão N"
N
N
Transistor NMOS
P

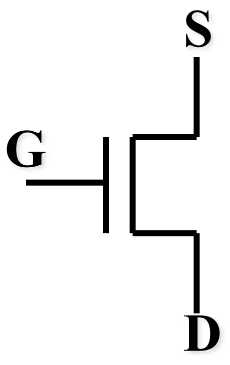

Fonte
Grade = VCC
canal "fechado"
Dreno
N
N
P



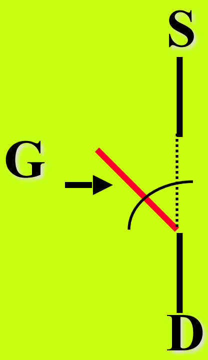
Funcionamento: através da carga colocada no gate (G), cargas de sentido oposto são atraídas para a interface com o óxido, formando o canal do transistor. Se estas cargas forem do mesmo tipo que as cargas presentes nas regiões de fonte (S) e dreno (D), haverá passagem de corrente (I) entre essas regiões através do canal do transistor.

Transistor NMOS

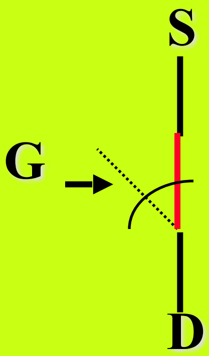
Símbolo:

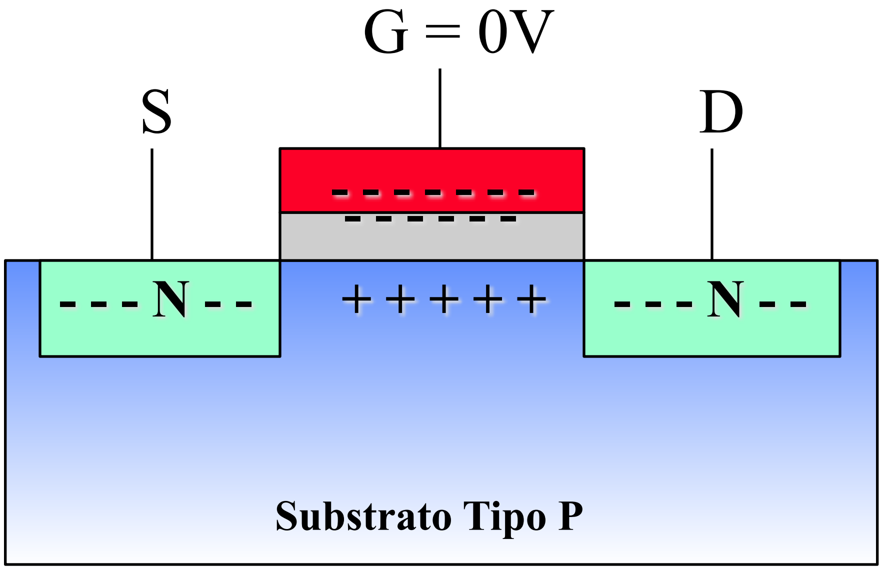


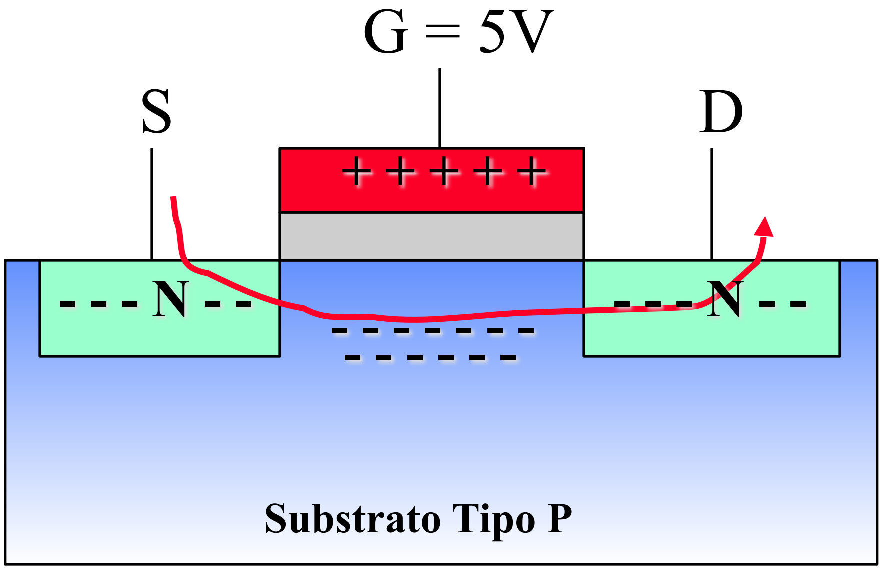
Se G = 0V ('0')
Chave aberta (off)



Se G = 5V ('1')
Chave fechada (on)

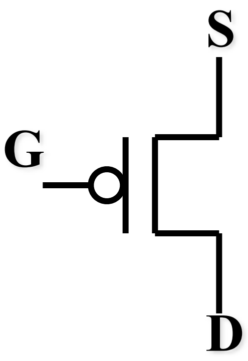



G = 0V
S
D
- - - - - - - -
- - - - - - -
- - - N - -
+ + + + + +
- - - N - -
Substrato Tipo P


G = 5V
S
D
+ + + + +
- - - N - -
- - - - - - -
- - - - - - -
- - - N - -
Substrato Tipo P

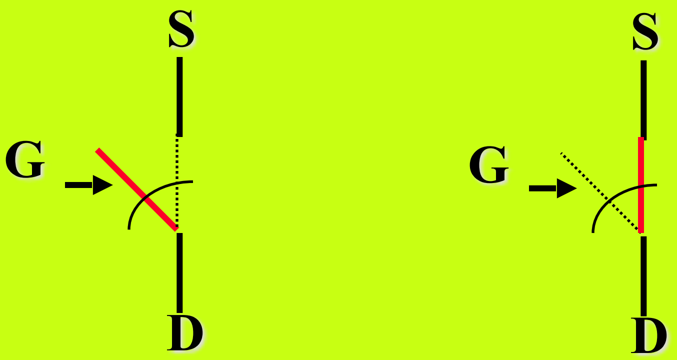
Transistor PMOS

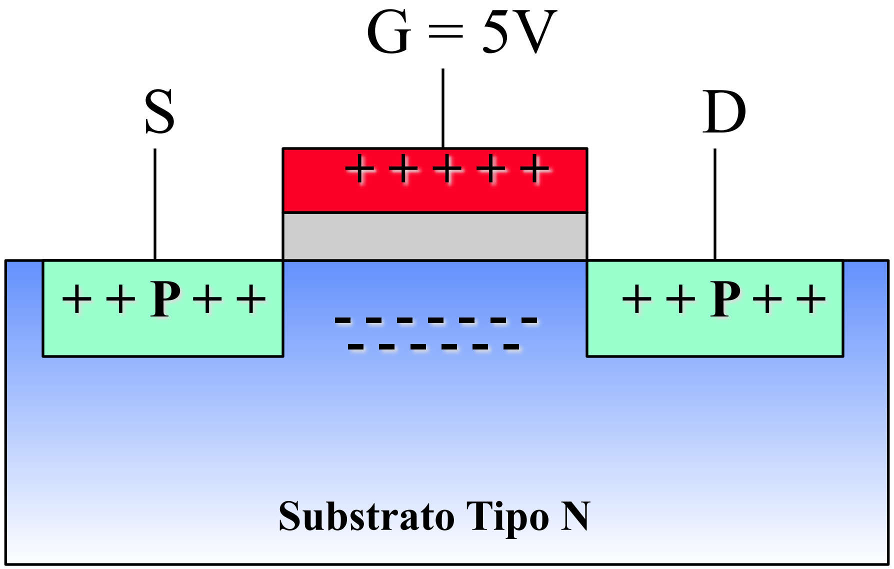
Símbolo:

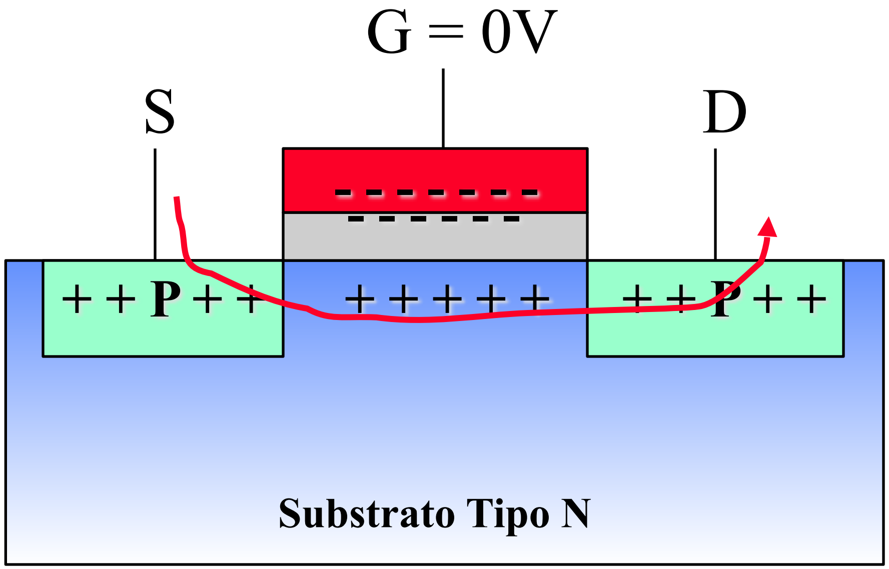


Se G = 5V ('1')
Chave aberta (off)

Se G = 0V ('0')
Chave fechada (on)



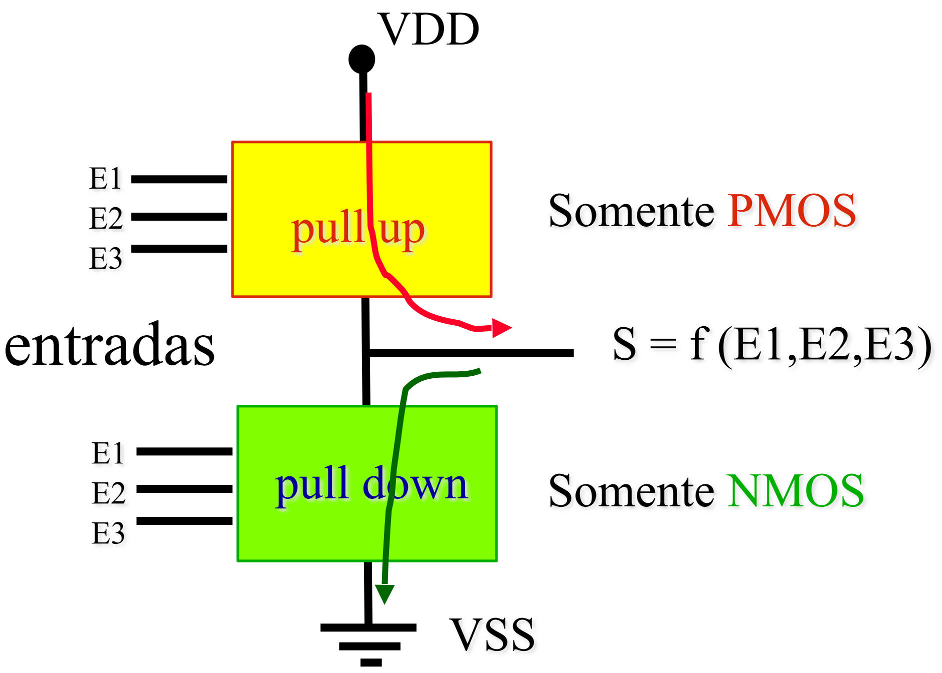

G = 5V
S
D
+ + + + + +
+ + P + +
+ + P + +
- - - - - - - -
- - - - - - -
Substrato Tipo N

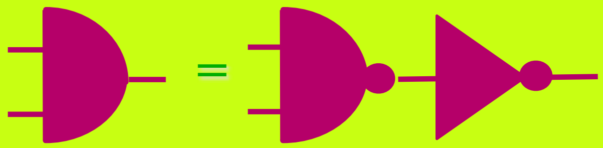

G = 0V
S
D
- - - - - - - -
- - - - - - -
+ + P + +
+ + + + + +
+ + P + +
Substrato Tipo N

Portas Lógicas

Circuitos CMOS Estáticos

De Morgan: $\overline{A + B} = \overline{A} \cdot \overline{B}$


VDD
E1
E2
E3
pull up
Somente PMOS
entradas
S = f (E1,E2,E3)
E1
E2
E3
pull down
Somente NMOS
VSS



AND = NAND + INV

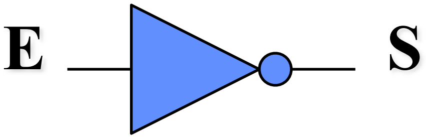
- A lógica PMOS permite conectar o sinal de saída a Vcc (5V), ‘1’ lógico.
- A lógica NMOS permite conectar o sinal de saída a Gnd (0V), ‘0’ lógico.
- Sempre um dos caminhos, para Vcc ou Gnd, estão fechados para a saída, conectando a mesma a 5V ou 0V.

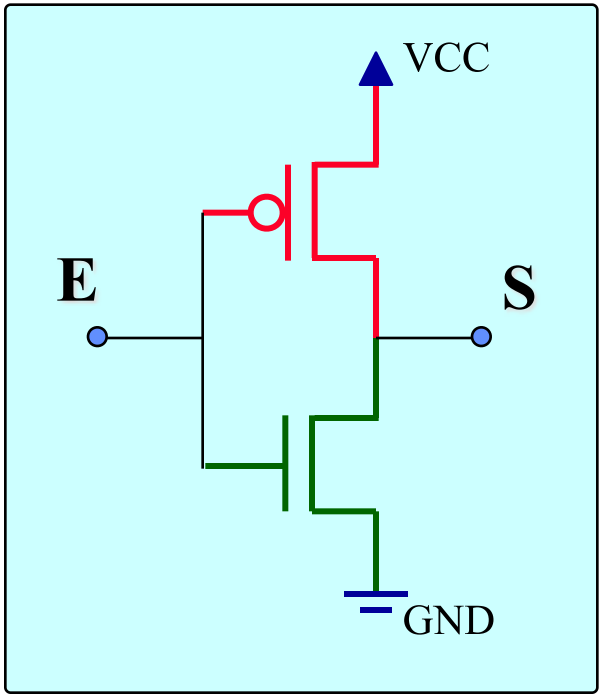
As redes PUP (pull up) e PDN (pull down) são duais nas suas topologias.

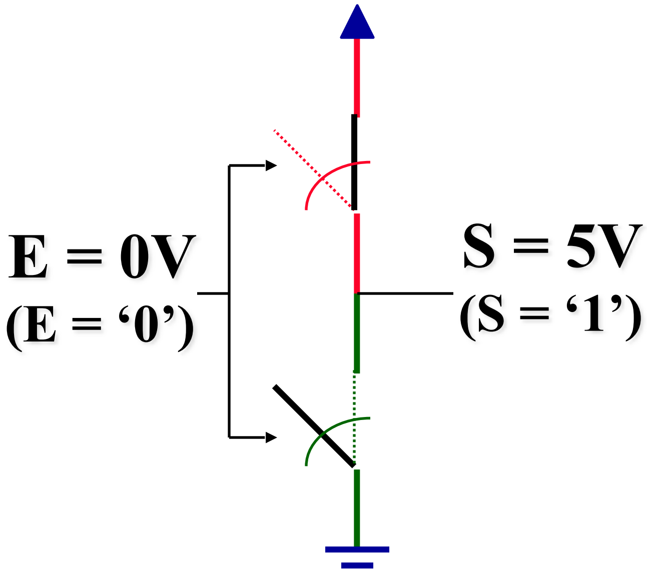
Portas Lógicas

INVERSOR CMOS

E	S
0	1
1	0

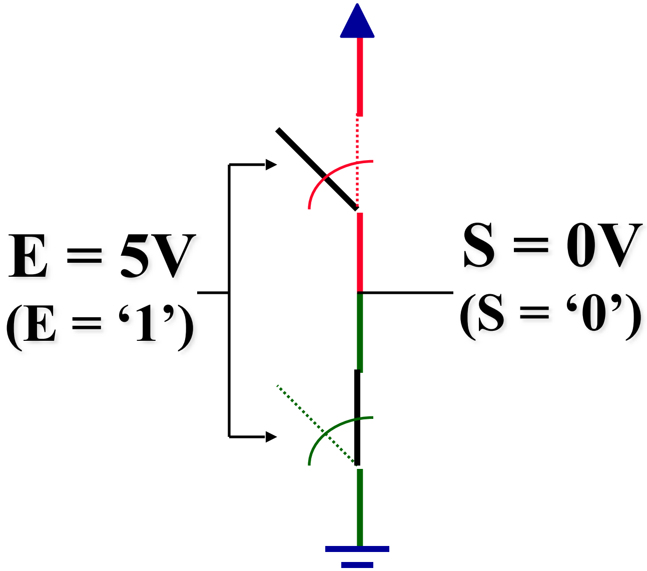






E = 0V
(E = ‘0’)

S = 5V
(S = ‘1’)



E = 5V
(E = ‘1’)

S = 0V
(S = ‘0’)

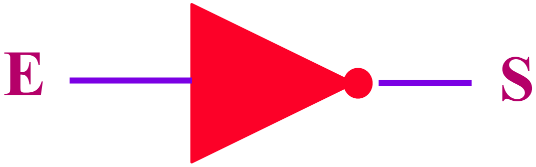
Portas Lógicas

INVERSOR CMOS

- **Equação:**

$$S = \overline{E}$$

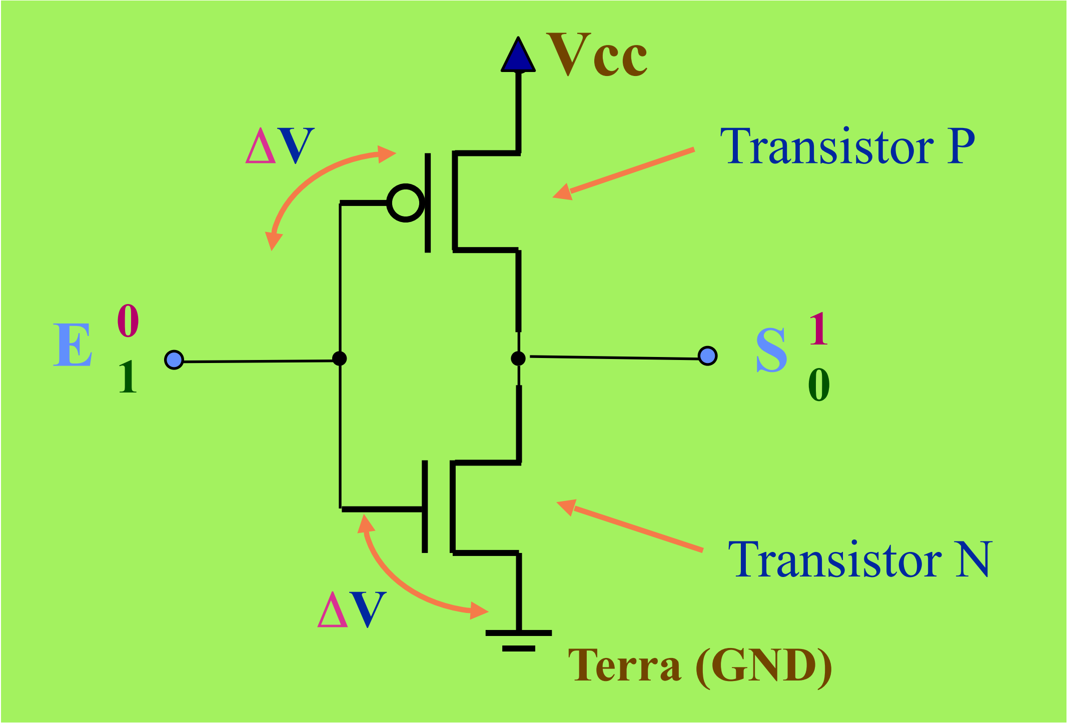
- **Esquema Lógico:**



- **Tabela Verdade:**

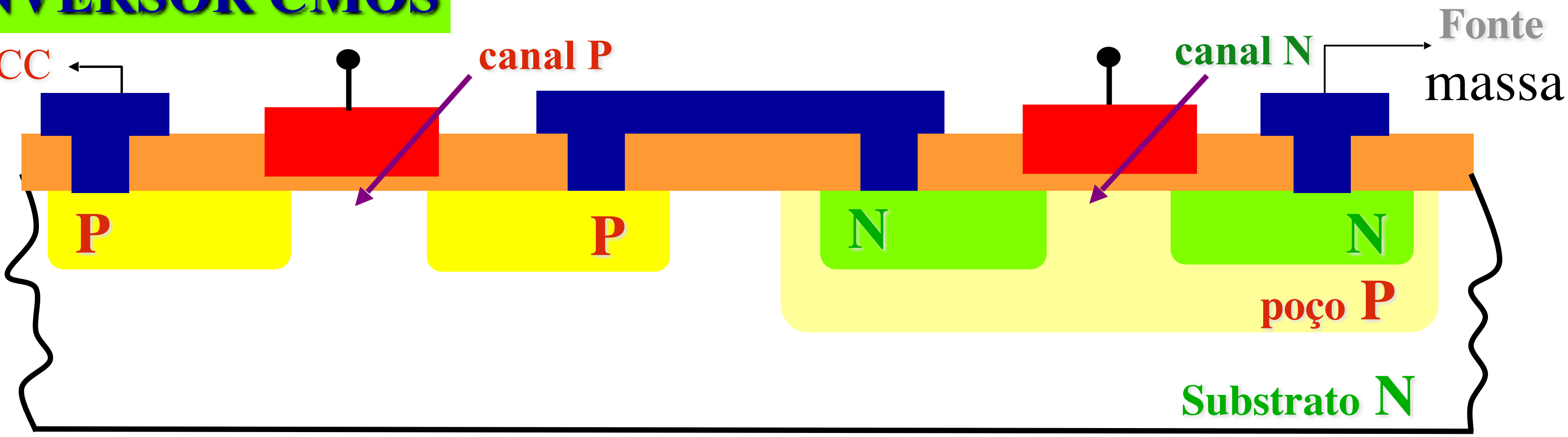
E	S
0	1
1	0

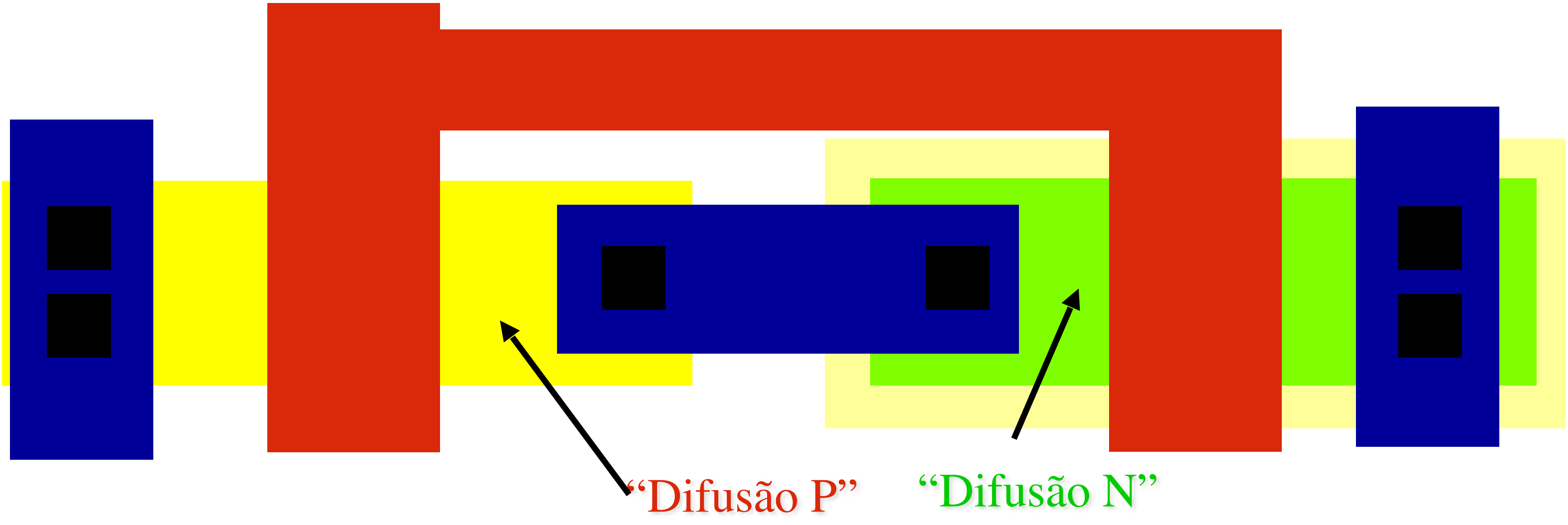
- **Esquema Elétrico CMOS**


Vcc
ΔV
Transistor P
E
0
1
S
1
0
Transistor N
ΔV
Terra (GND)

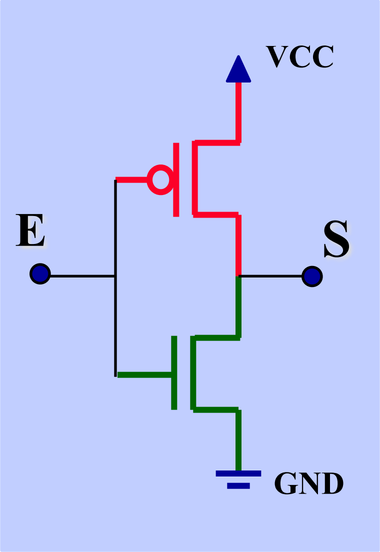
Portas Lógicas

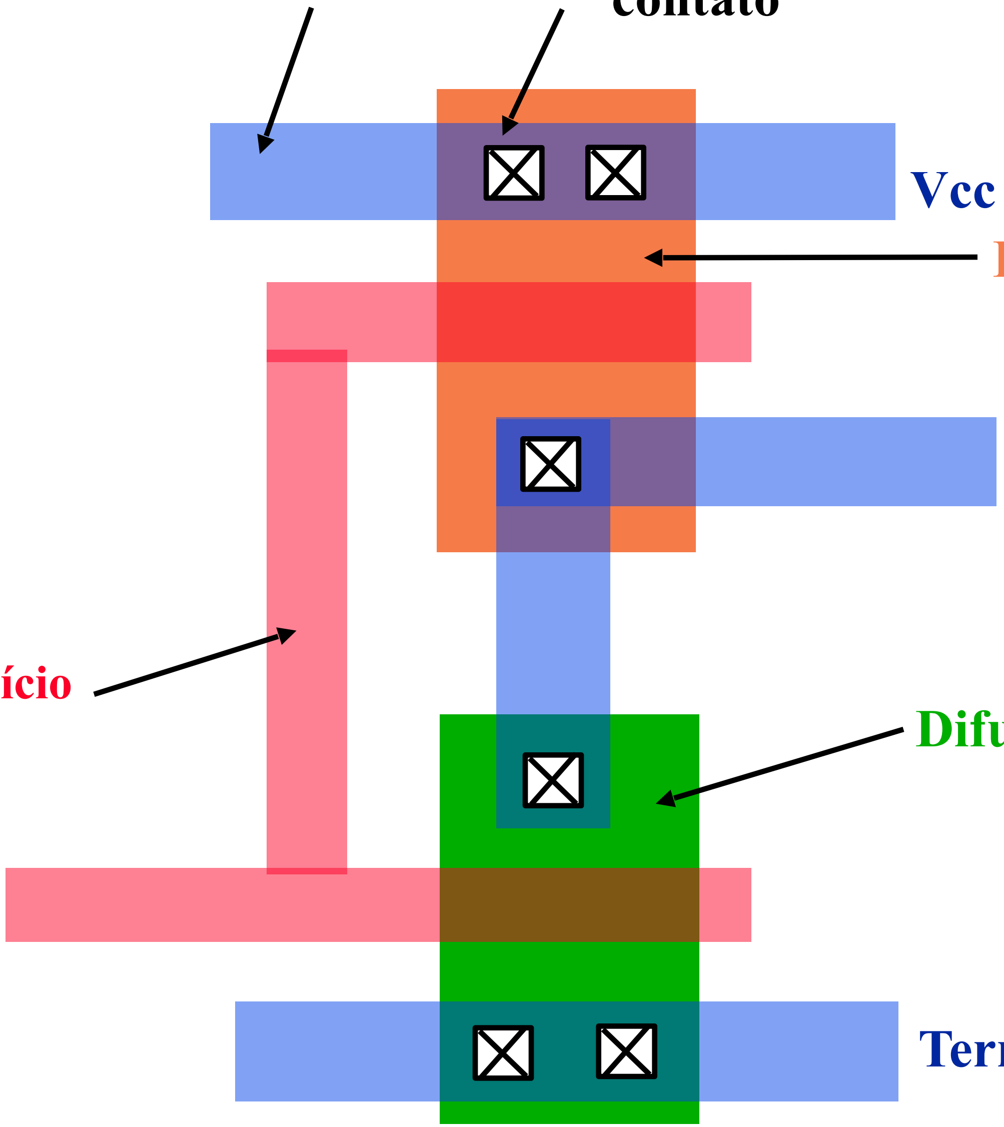
INVERSOR CMOS


VCC
canal P
canal N
Fonte
massa
P
P
N
N
poço P
Substrato N


"Difusão P"
"Difusão N"

LAYOUT DO INVERSOR CMOS





metal

contato

Vcc

Difusão P

Saída

Polisilício

Difusão N

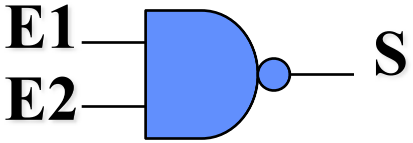
E

Terra

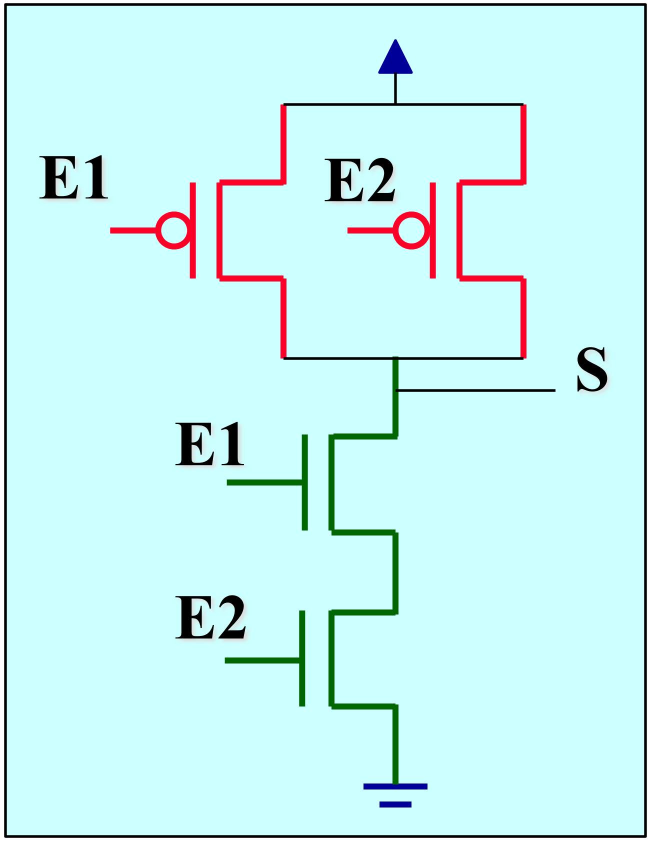
$$S = \overline{E}$$

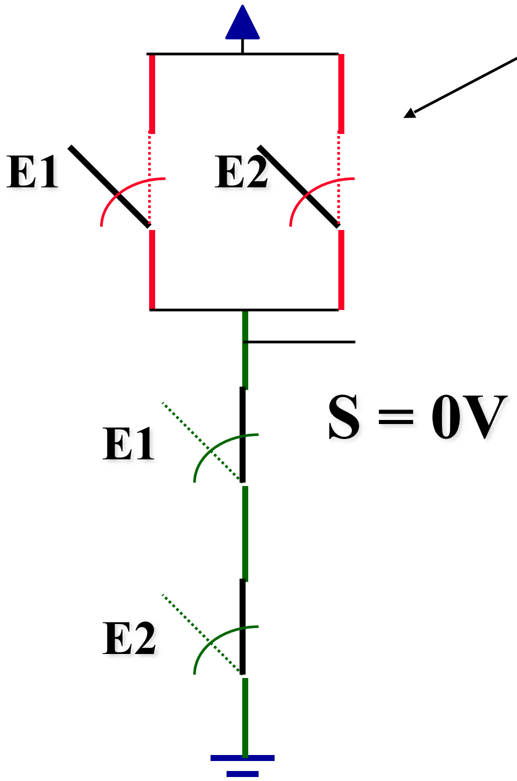
Portas Lógicas

Porta NAND CMOS



E1	E2	S
0	0	1
0	1	1
1	0	1
1	1	0




E1
E2
S = 0V
E1
E2

Dica: A SAÍDA É 0 SOMENTE QUANDO TODAS AS ENTRADAS FOREM 1, CASO CONTRÁRIO HAVERÁ 1 NA SAÍDA. CONTRÁRIO DA PORTA ‘AND’.

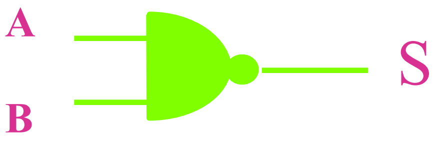
Portas Lógicas

Porta NAND CMOS

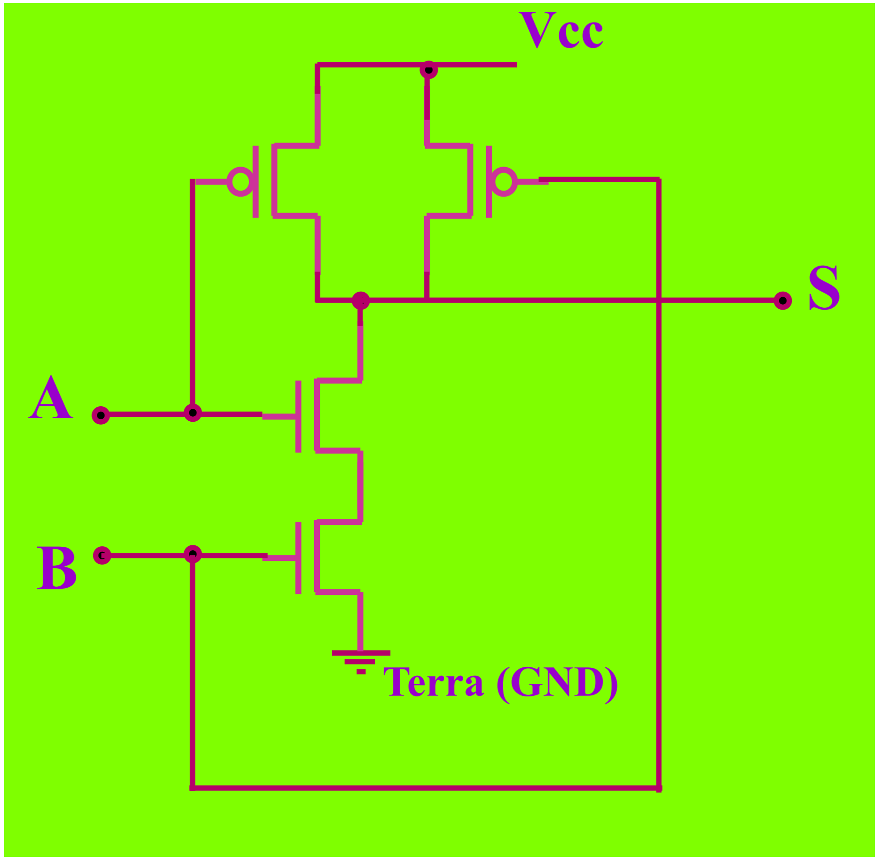
- Equação Lógica:

$$S = \overline{A \cdot B}$$

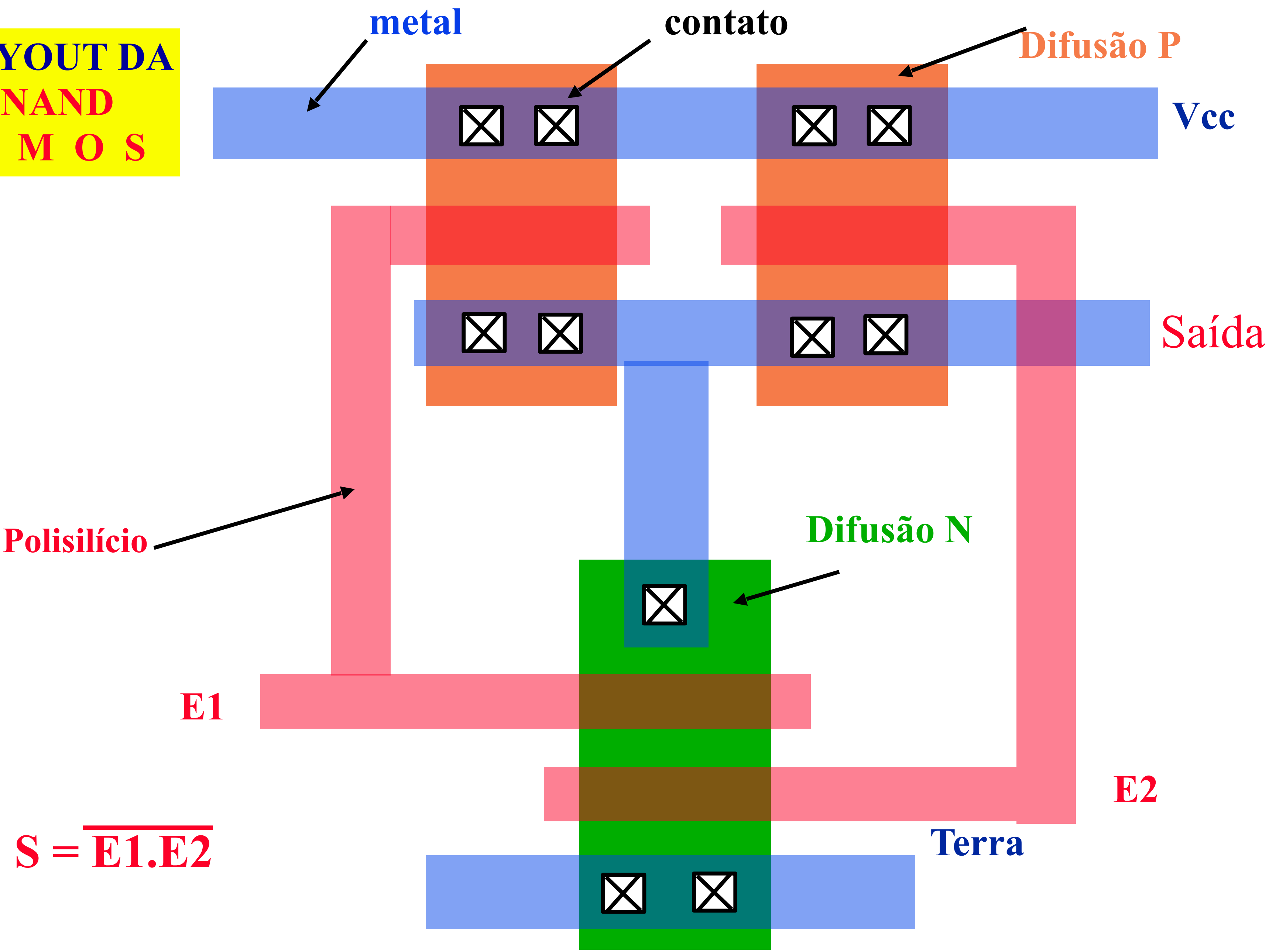
- Esquema Lógico :



- Esquema Elétrico:


Vcc
S
A
B
Terra (GND)

LAYOUT DA NAND C M O S

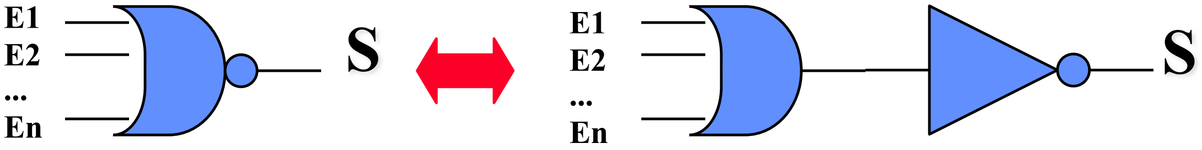

metal
contato
Difusão P
Vcc
Saída
Polisilício
Difusão N
E1
E2
Terra

$$S = \overline{E1.E2}$$

Portas Lógicas

Porta NOR CMOS

Símbolo:



Equação Booleana: $S = \overline{E1 + E2}$

$$S = \overline{E1 + E2 + \dots + En}$$

Tabela Verdade:

E1	E2	S
0	0	1
0	1	0
1	0	0
1	1	0

E1	E2	...	En	S
0	0		0	1
0	1		0	0
1	0		0	0
1	1	...	1	0

Dica: A SAÍDA É 1 SOMENTE QUANDO TODAS AS ENTRADAS FOREM 0, CASO CONTRÁRIO HAVERÁ 0 NA SAÍDA. OU SEJA, 1 EM UMA DAS ENTRADAS JÁ GARANTE 0 NA SAÍDA. CONTRÁRIO DA PORTA OR.

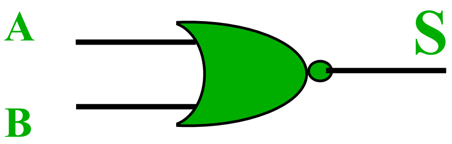
Portas Lógicas

Porta NOR CMOS

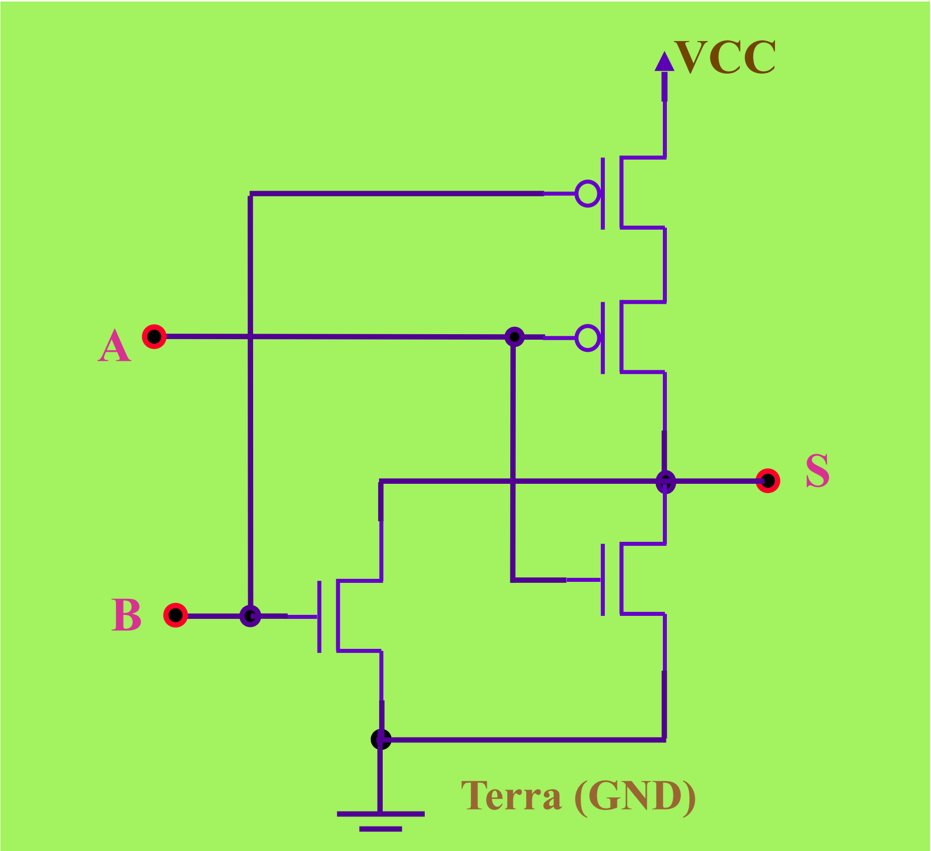
- **Equação:**

$$S = \overline{A + B}$$

- Esquema Lógico:



- **Esquema Elétrico CMOS**


VCC
A
B
S
Terra (GND)