INF01058

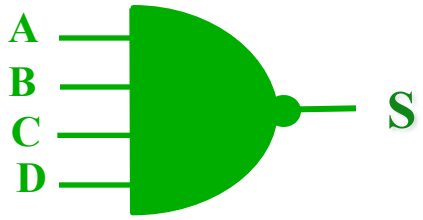
Circuitos Digitais

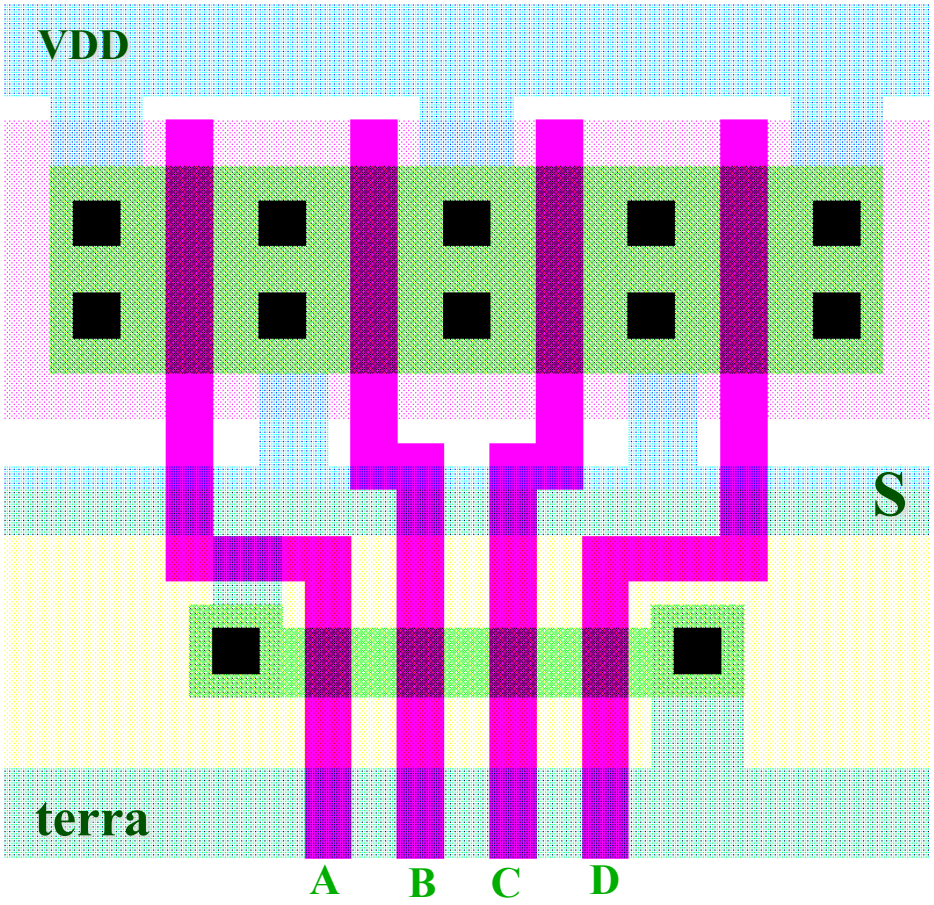
Portas Complexas
Lógica com Chaves
Transmission Gates

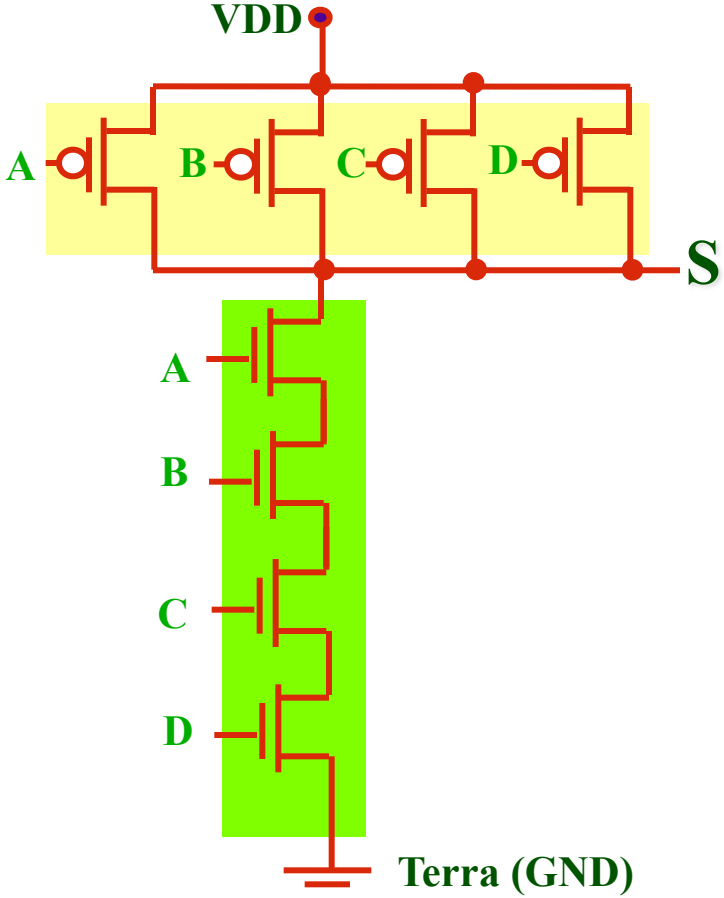
Aula 2b

Portas Lógicas

Porta NAND CMOS



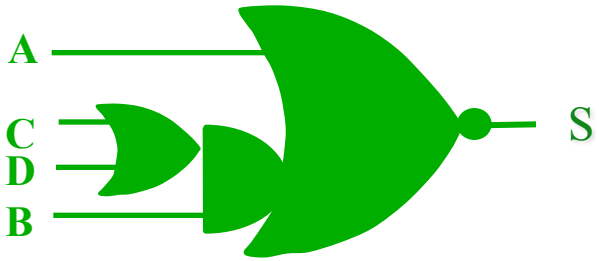




Portas Lógicas

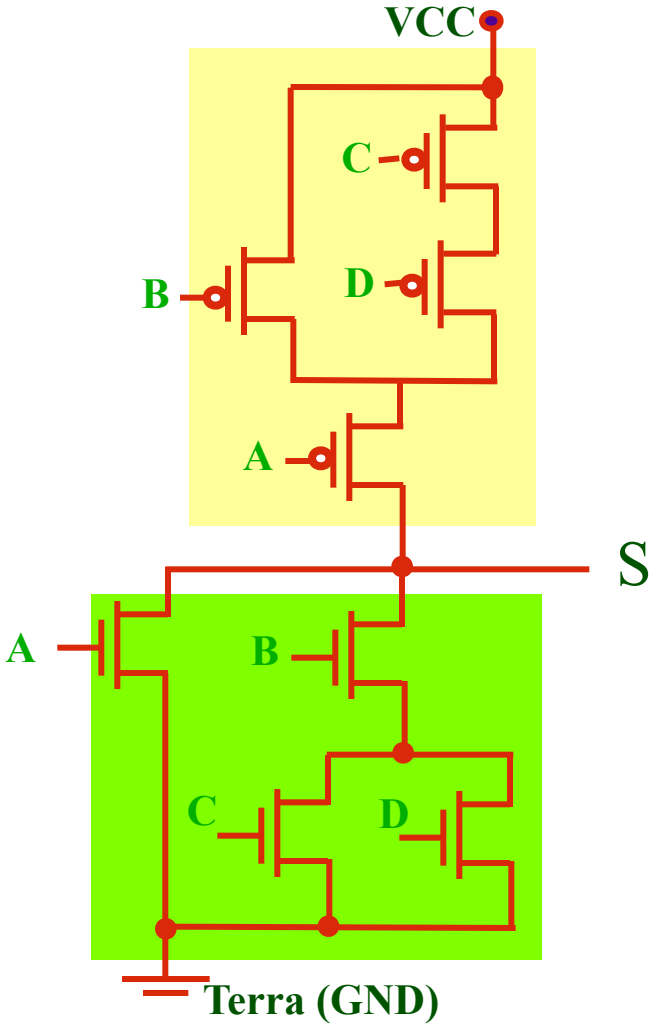
Portas CMOS Complexas
SCCG (Static CMOS Complex Gate)

Exemplo:



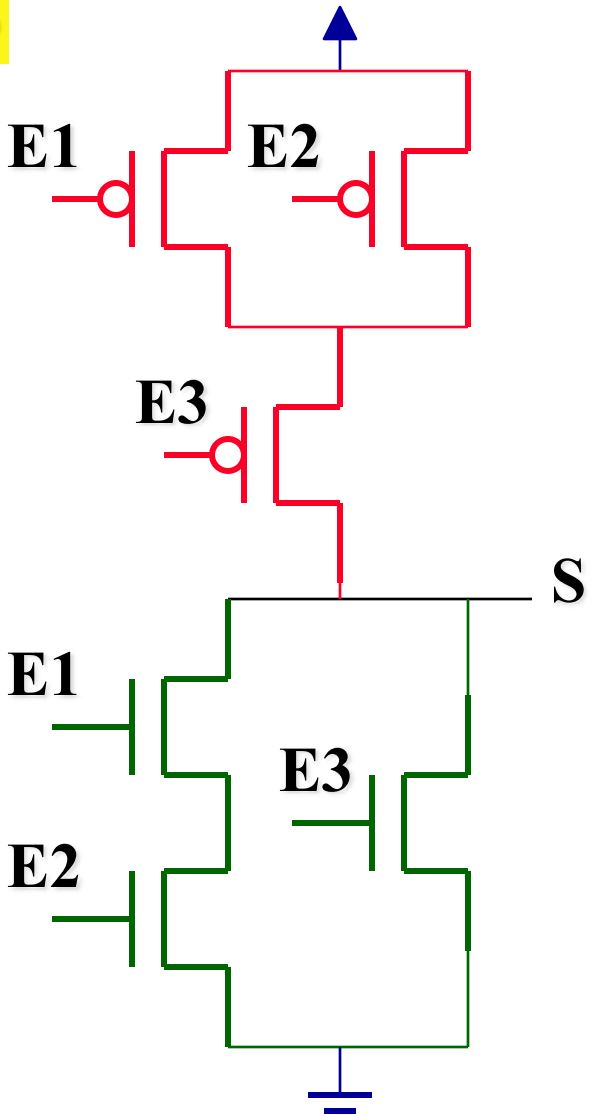
$$S = \overline{A + (B \,.(C+D))}$$

O funcionamento complementar das redes (P e N) é definido pela topologia dual das redes de "*pull up*" e de "*pull down*".

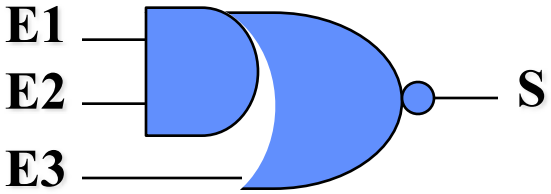


Portas Lógicas

Exercício

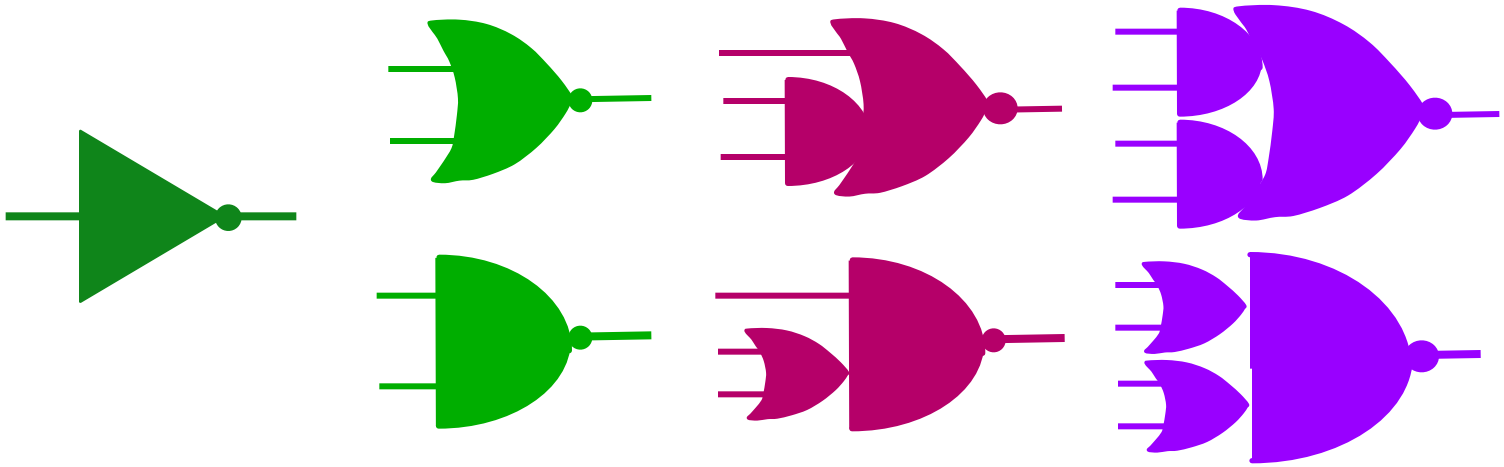


E1	E2	E3	S
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0



Portas Lógicas

Portas CMOS Complexas
SCCG (Static CMOS Complex Gate)



Exemplo: Funções com até 2 transistores em série

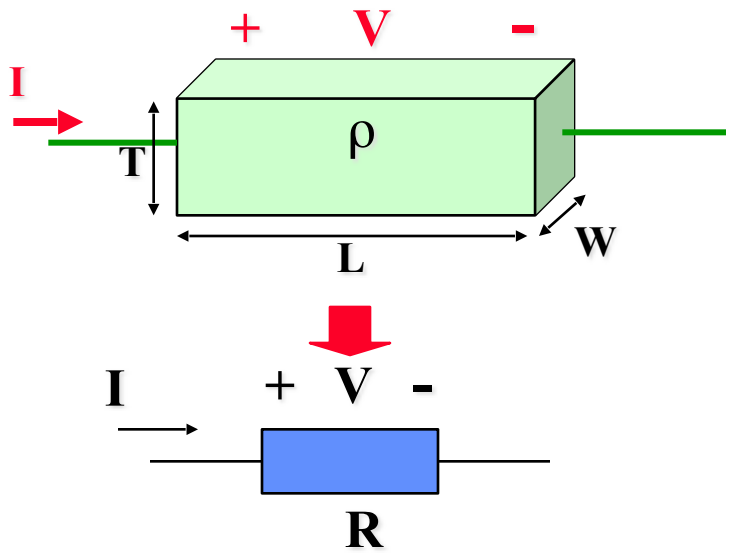
Dimensionamento de Transistor MOS

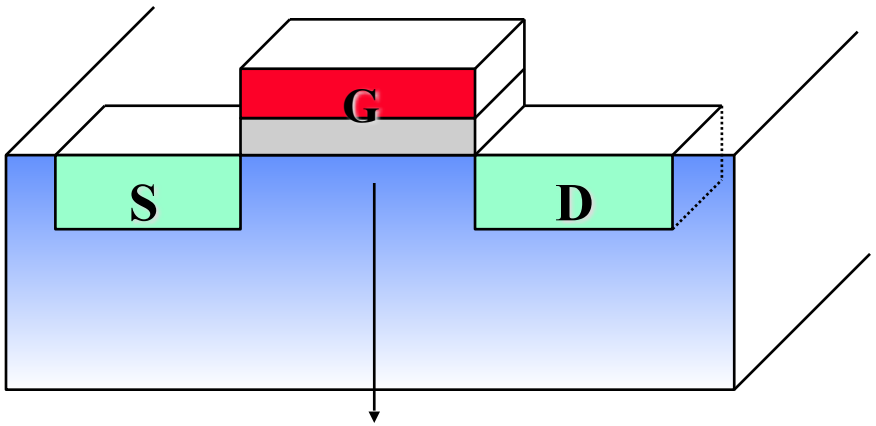
Revisão de Resistência

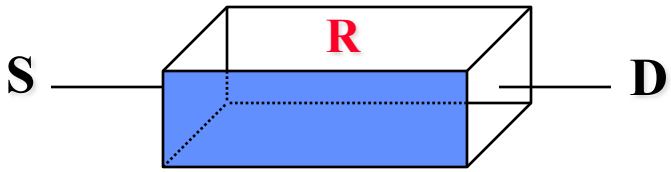
$$R = \rho \cdot \frac{L}{W \cdot T}$$

Lei de Ohm:

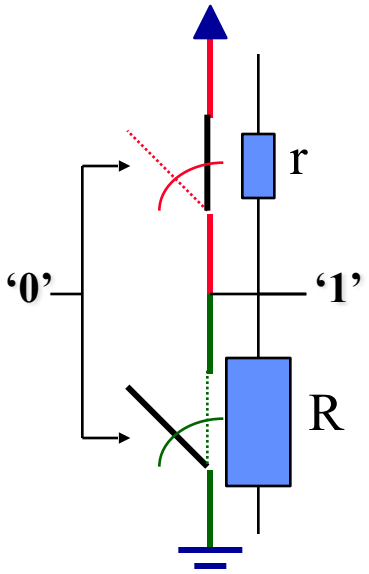
$$I = V / R$$



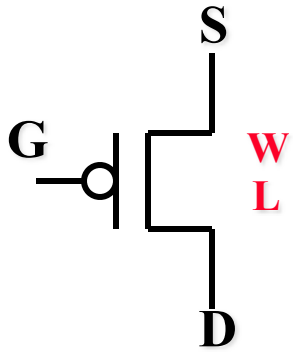




canal do transistor

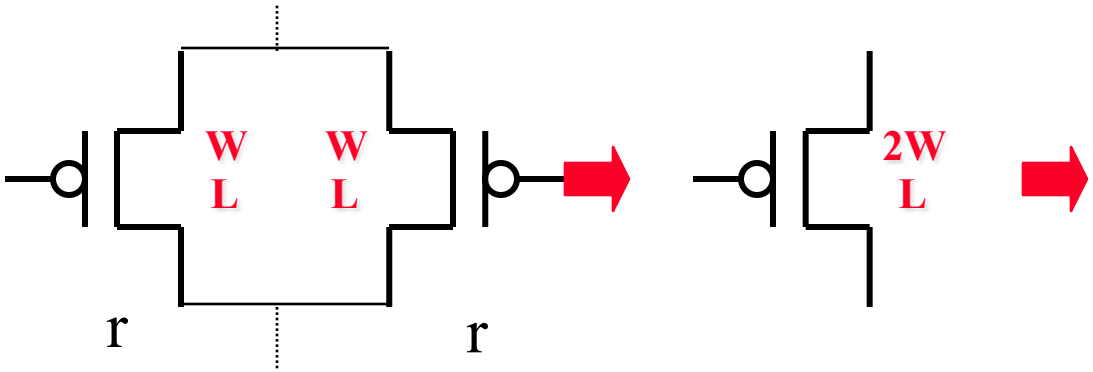


$$\begin{cases} W \uparrow : r \downarrow, C \uparrow \\ L \uparrow : r \uparrow, C \uparrow \end{cases}$$

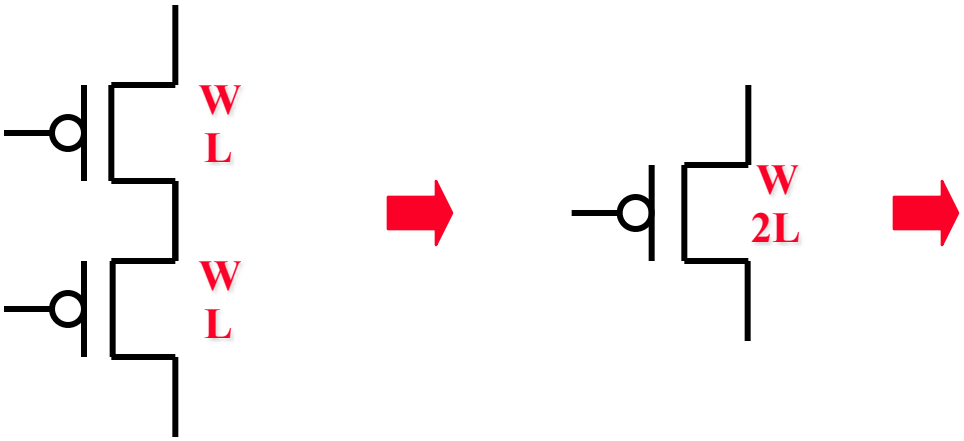


Associação de Transistores

Transistores em Paralelo



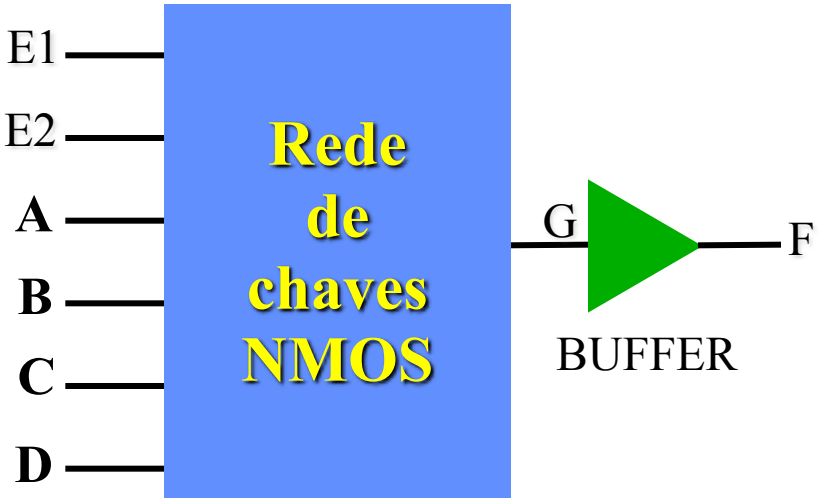
Transistores em Série

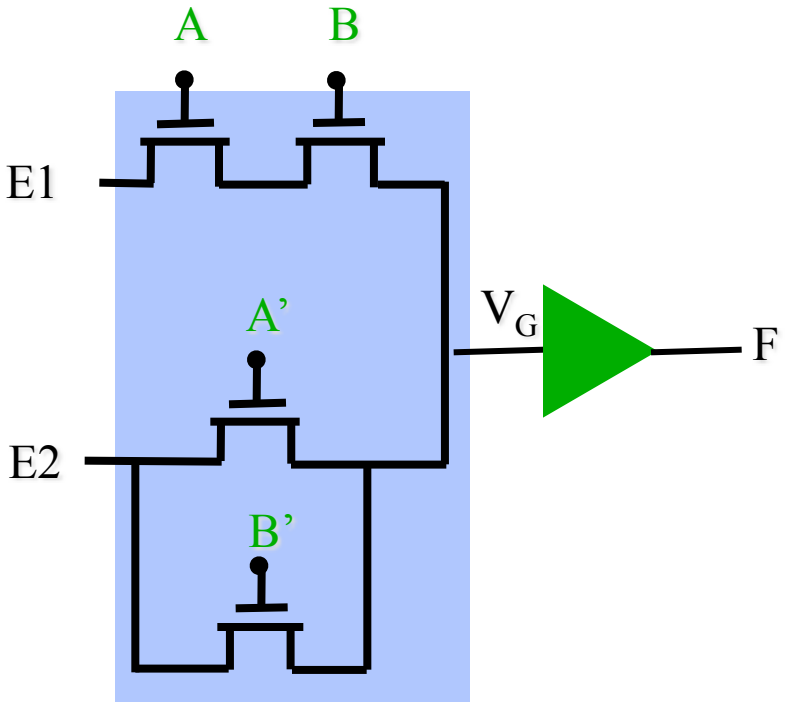


* Mais de 4 transistores em série devem ser evitados !!!

Portas Lógicas

Lógica com chaves NMOS





Transistores N

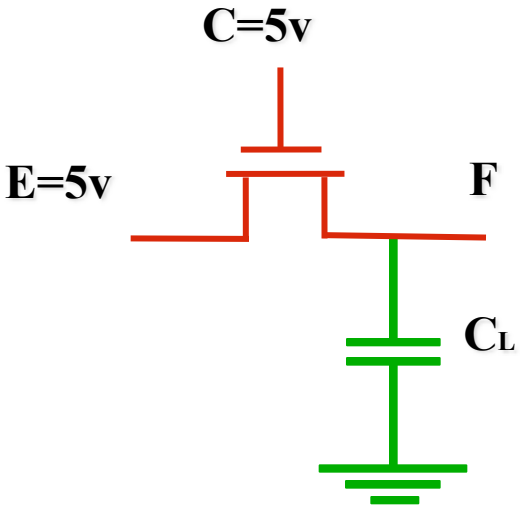
Sem consumo estático na rede de chaves.

V_G alto varia em função da lógica.

O buffer regenera o sinal lógico.

Portas Lógicas

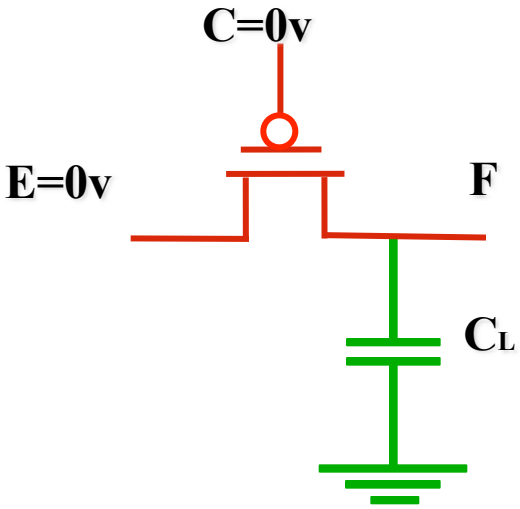
Chaves NMOS



- V_F está abaixo de V_C para NMOS "ON"
- V_F não consegue atingir **5V**, mas **5V** $-V_{Tn}$
- O transistor NMOS passa um '0' forte (GND) e um '1' fraco ($V_C - V_{Tn}$)

Portas Lógicas

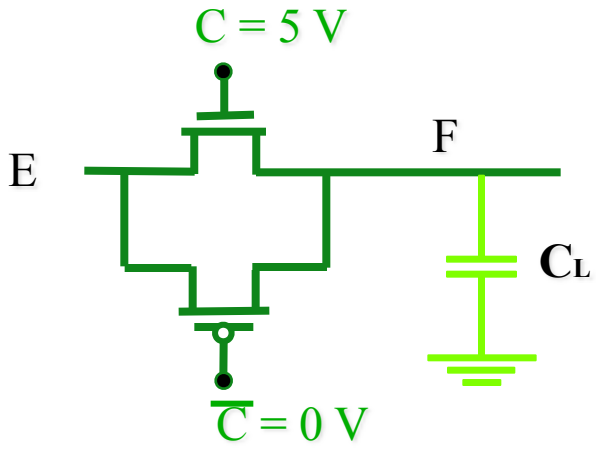
Chaves PMOS



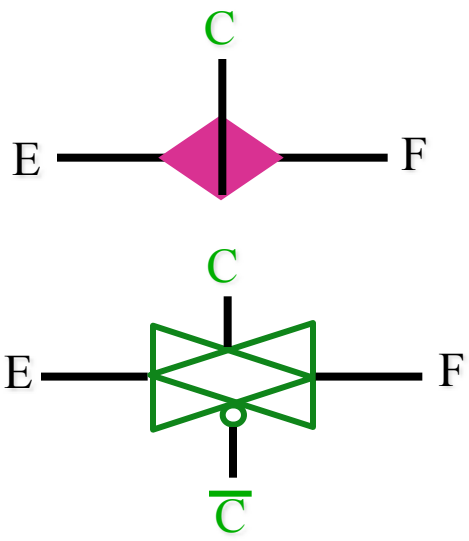
- V_F está acima de V_C para PMOS "ON"
- V_F não consegue atingir 0V, mas V_{Tn}
- O transistor PMOS passa um '1' forte (VCC) e um '0' fraco ($+V_{Tn}$)

Portas Lógicas

Chaves CMOS



Símbolos:



OBS: o transistor PMOS passa um ‘0’ fraco e um ‘1’ forte

o transistor NMOS passa um ‘0’ forte e um ‘1’ fraco

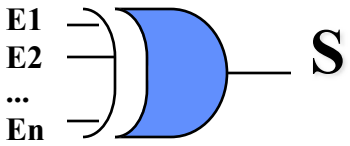
R_{eq} de uma chave CMOS: cerca de 10 KΩ

Desvantagem: A chave é controlada por C e $\overline{C}$

Portas Lógicas

Porta XOR (porta 'OU Exclusivo')

Símbolo:



Equação Booleana: $S = E1 \oplus E2$

$S = E1 \oplus E2 \oplus ... \oplus En$

Tabela Verdade:

E1	E2	S
0	0	0
0	1	1
1	0	1
1	1	0

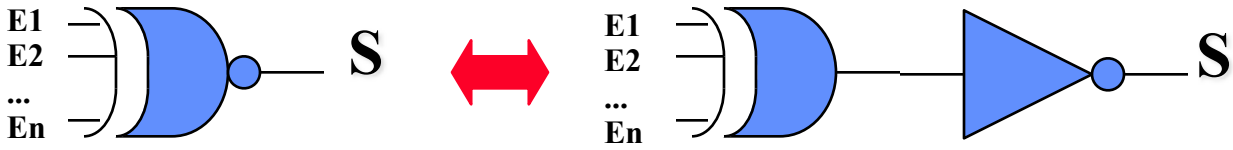
E1	E2	...	En	S
0	0		0	0
0	1		1	0
1	0		0	1
1	1	...	1	1

Dica: A SAÍDA É 1 SOMENTE QUANDO HOUVER UM NÚMERO ÍMPAR DE ENTRADAS COM VALOR 1.

Portas Lógicas

XNOR (porta 'Não OU Exclusivo')

Símbolo:



Equação Booleana: $S = \overline{E1 \oplus E2}$

$S = \overline{E1 \oplus E2 \oplus \ldots \oplus En}$

Tabela Verdade:

E1	E2	S
0	0	1
0	1	0
1	0	0
1	1	1

E1	E2	...	En	S
0	0		0	1
0	1		1	1
1	0		0	0
1	1	...	1	0

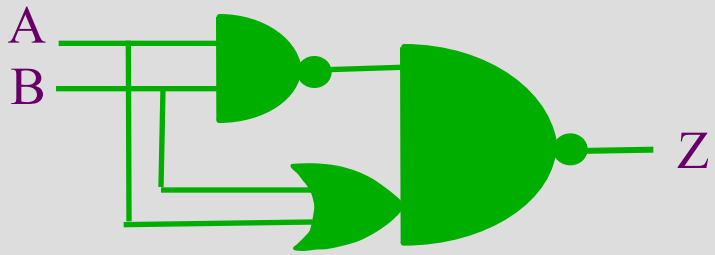
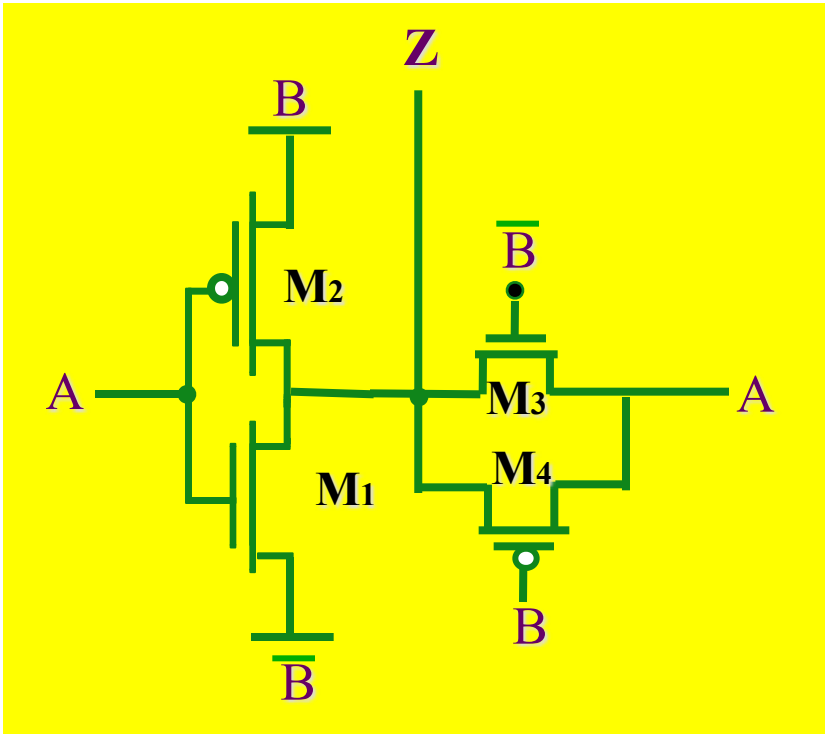
Dica: A SAÍDA É 1 SOMENTE QUANDO HOUVER UM NÚMERO PAR DE ENTRADAS COM VALOR 1. CONTRÁRIO DA PORTA XNOR.

Portas Lógicas

Lógica com chaves CMOS

XNOR e XOR

XNOR realizado com portas lógicas



XOR realizado com transistores de passagem