INF01058

# Circuitos Digitais

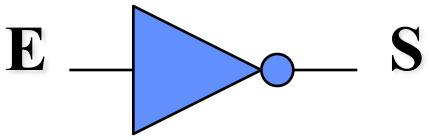
Resumo
Parasitas RC em Portas CMOS
Alta Impedância

Aula 4a

# Portas Lógicas (revisão ...)

**INV**

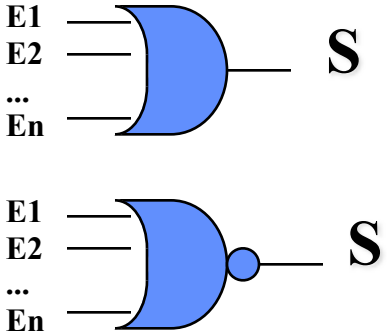
$E = \overline{S}$




| E | INV |
|---|---|
| 0 | 1 |
| 1 | 0 |

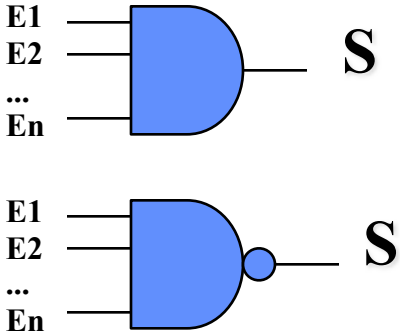
**OR (NOR)**

$S = E1 + E2$



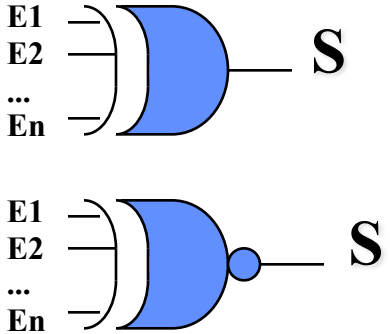

**AND (NAND)**

$S = E1 \bullet E2$




**XOR (XNOR)**

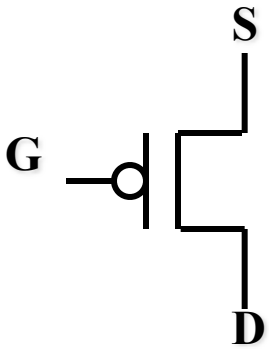
$S = E1 \oplus E2$



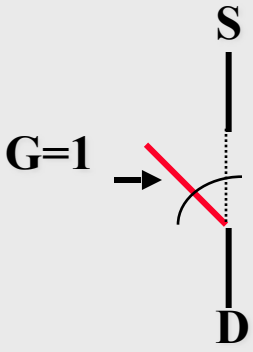

| E1 | E2 | AND | NAND | OR | NOR | XOR | XNOR |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |

# Transistores PMOS e NMOS (revisão ...)

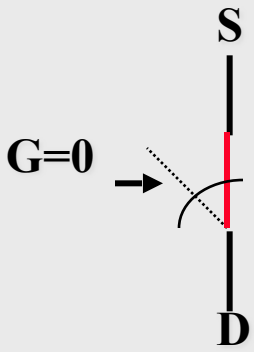
PMOS:



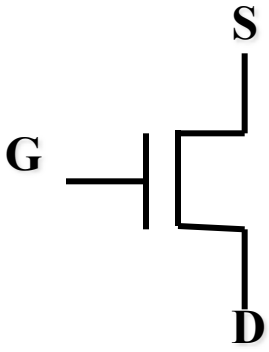

Se G = 5V (‘1’)
*Chave aberta (off)*



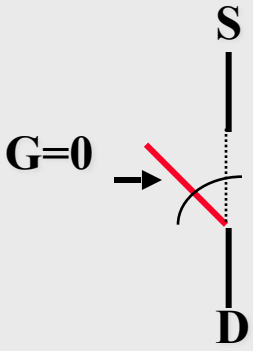

Se G = 0V (‘0’)
*Chave fechada (on)*



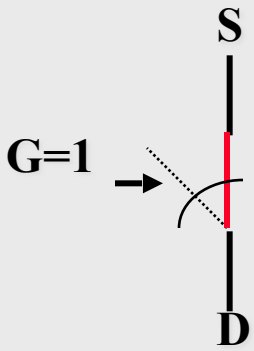

NMOS:



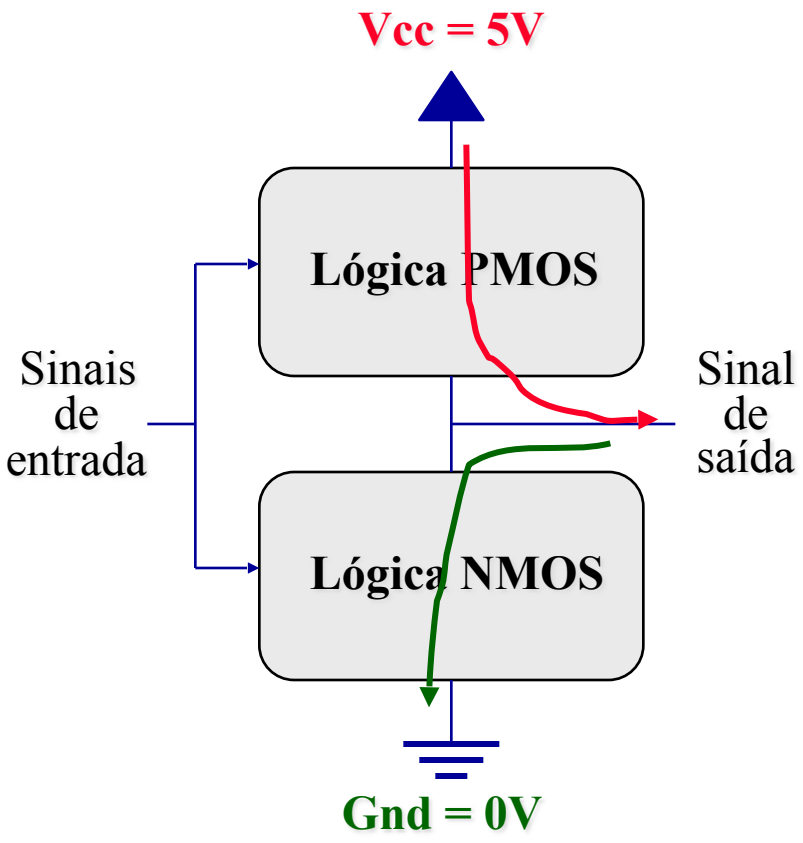

Se G = 0V (‘0’)
*Chave aberta (off)*

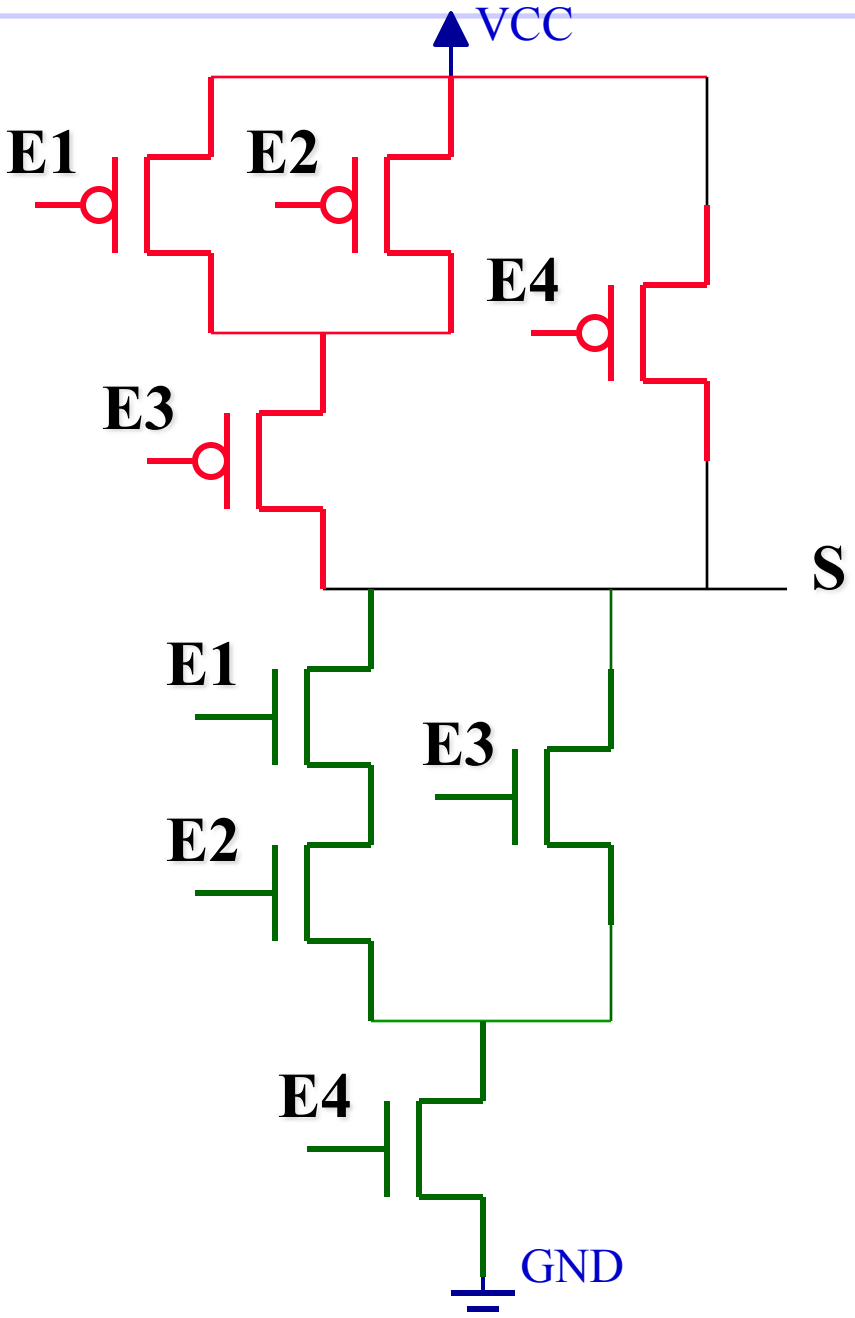



Se G = 5V (‘1’)
*Chave fechada (on)*



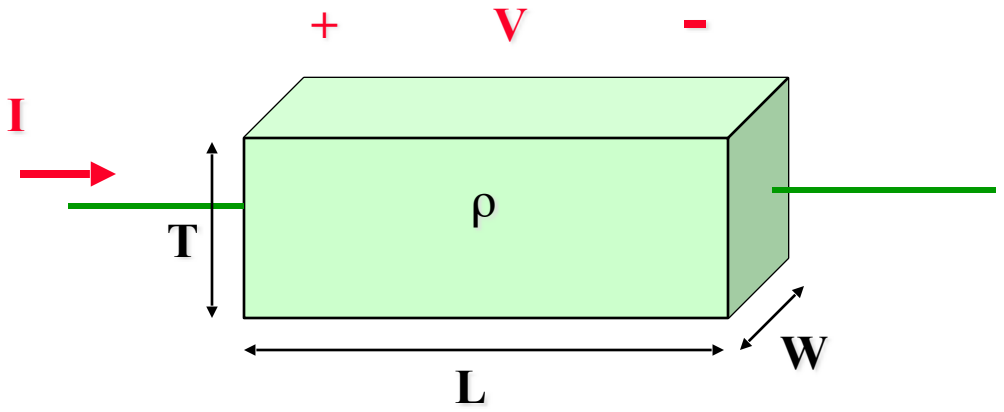
# Porta Lógica CMOS (revisão)



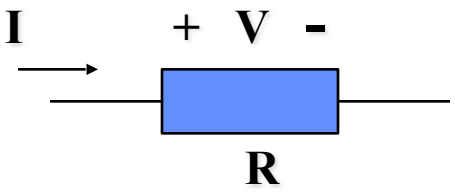
# Resistência (R)

$$R = \rho \cdot \frac{L}{W \cdot T}$$

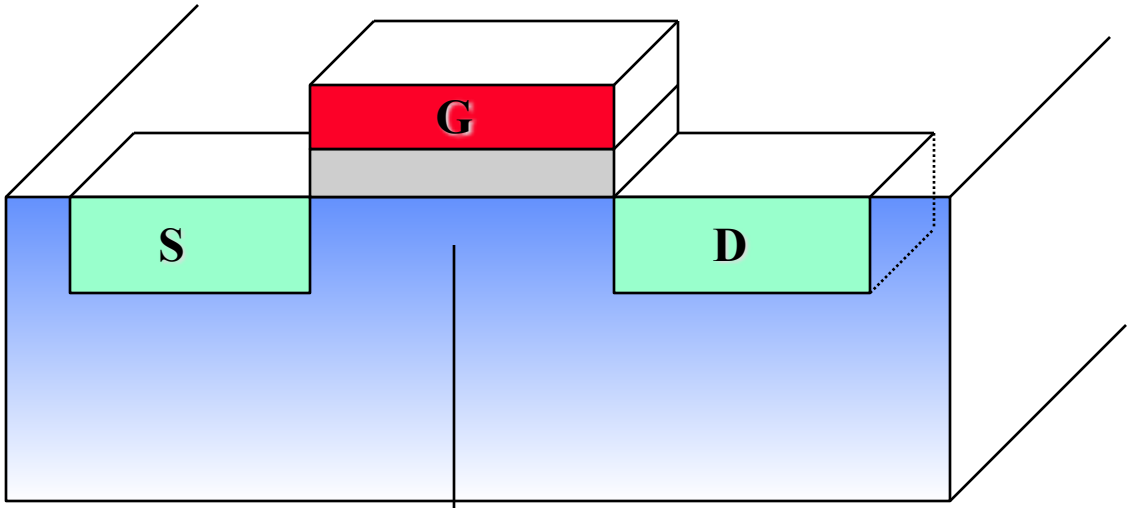


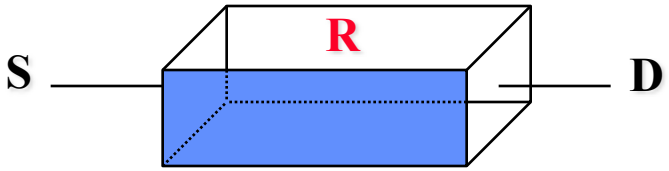

Lei de Ohm:

$$R = V / I$$



# Resistência de Canal do Transistor



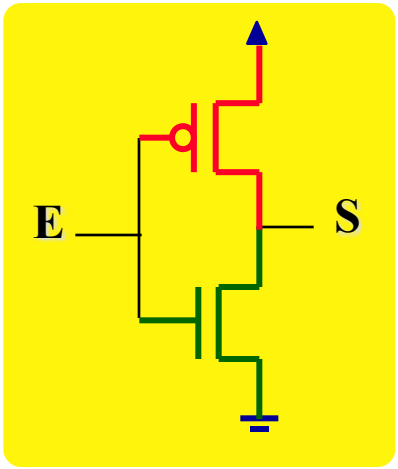

*canal do transistor*

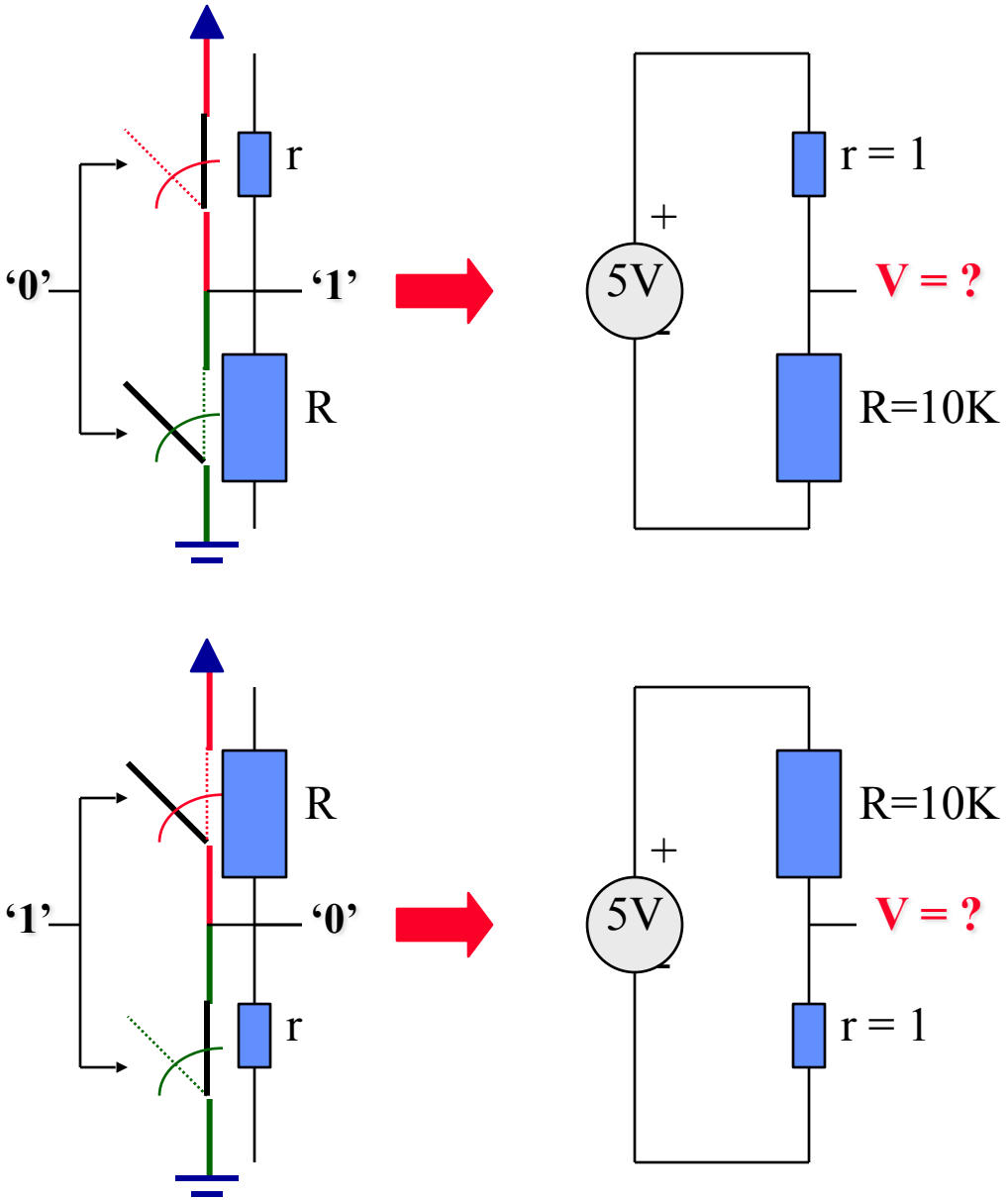
- Transistor não é 'chave ideal'.
- Canal do transistor ⇒ resistência
- Transistor conduzindo:

  resistência pequena ($R \Rightarrow 0$)
- Transistor 'cortado':

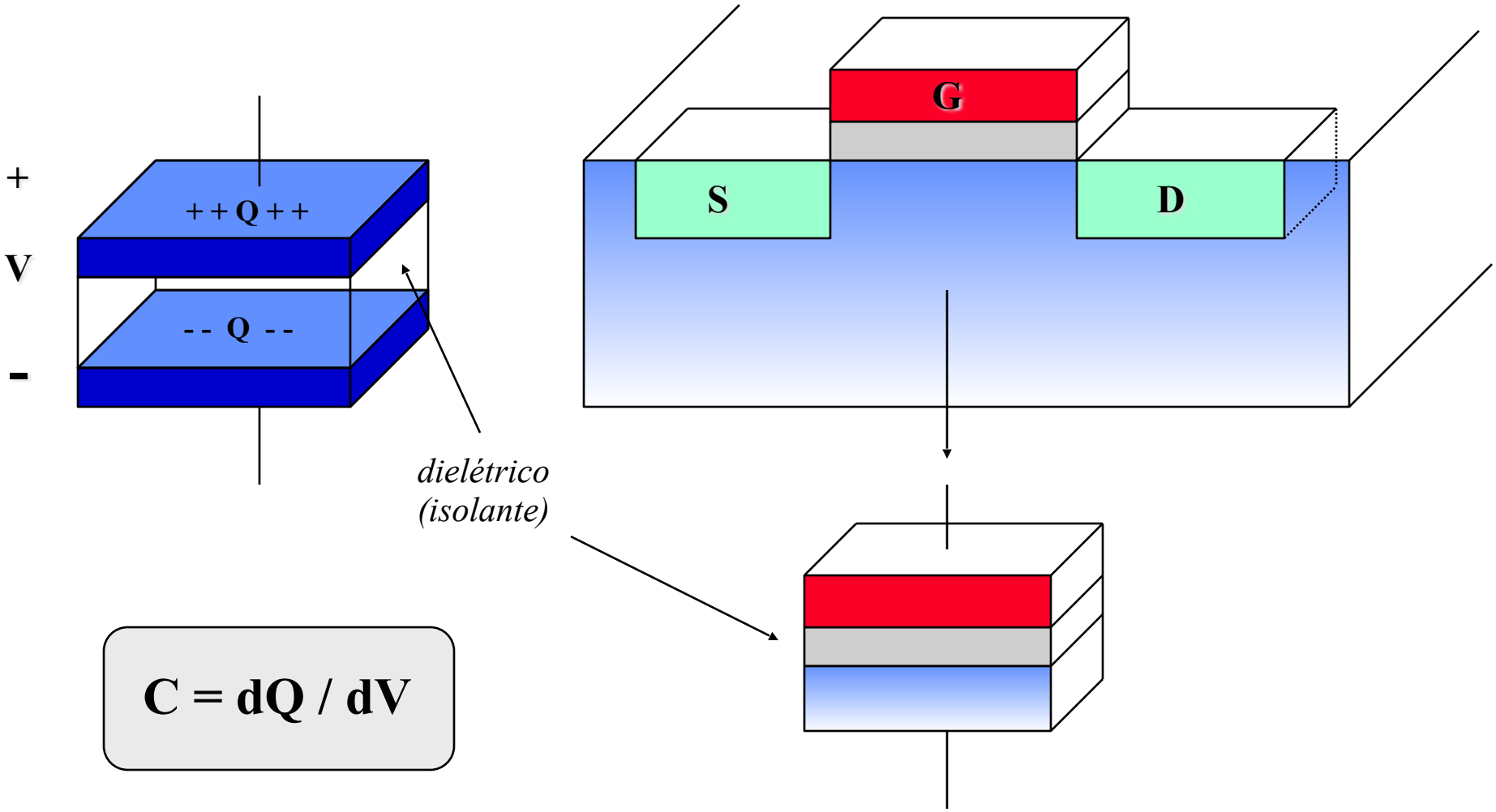
  resistência muito alta ($R \Rightarrow \infty$)

# Inversor CMOS : (resistência parasita)



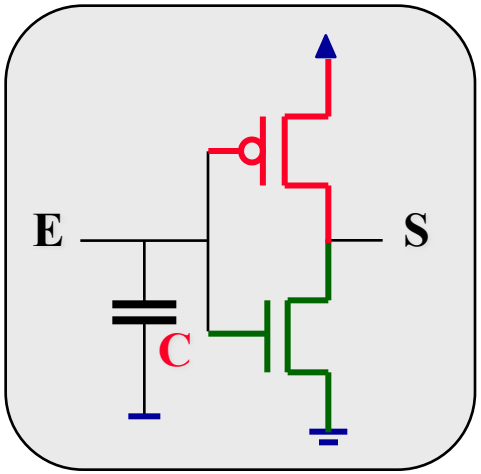



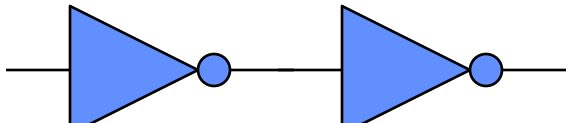
# Capacitância (C)

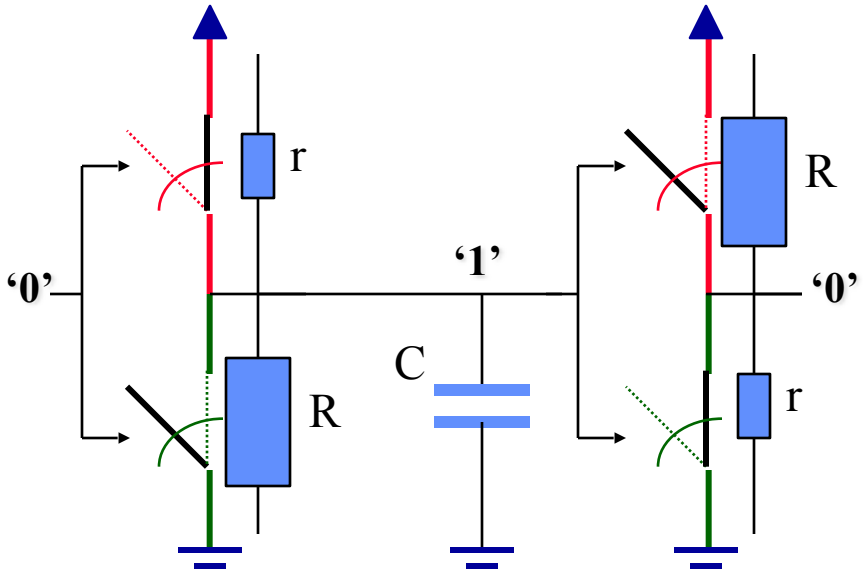


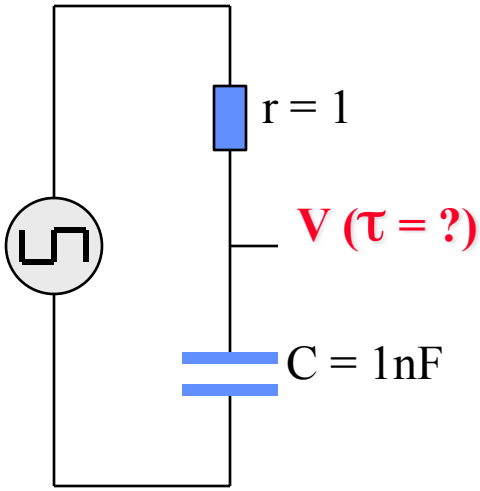

$$C = dQ / dV$$

# Inversor CMOS : (capacitância parasita)



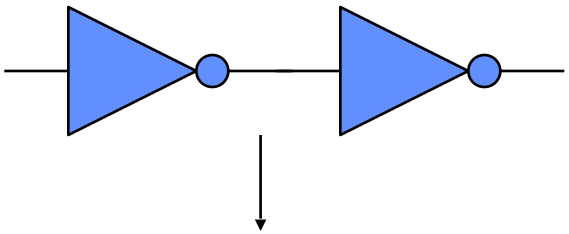





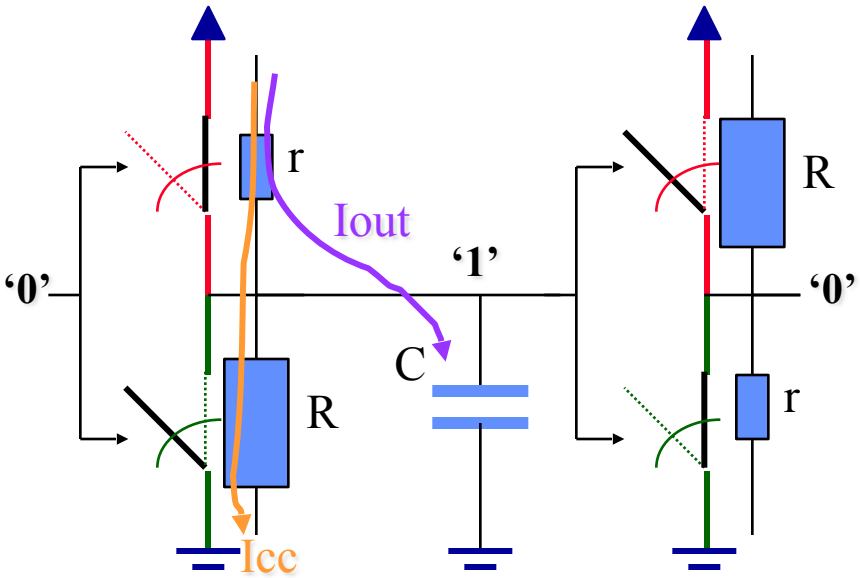



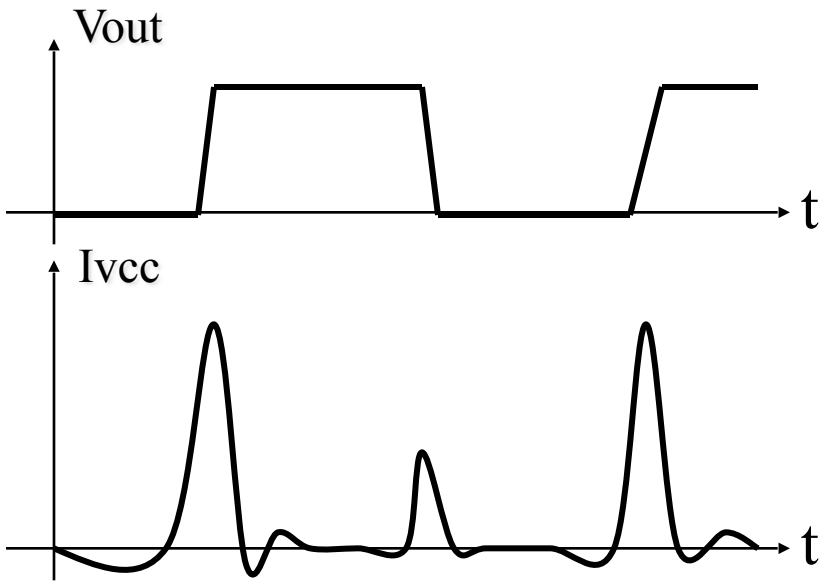
# Consumo (Dissipação de Potência)

- Corrente de Carga: Iout
- Corrente de Curto-Circuito: Icc



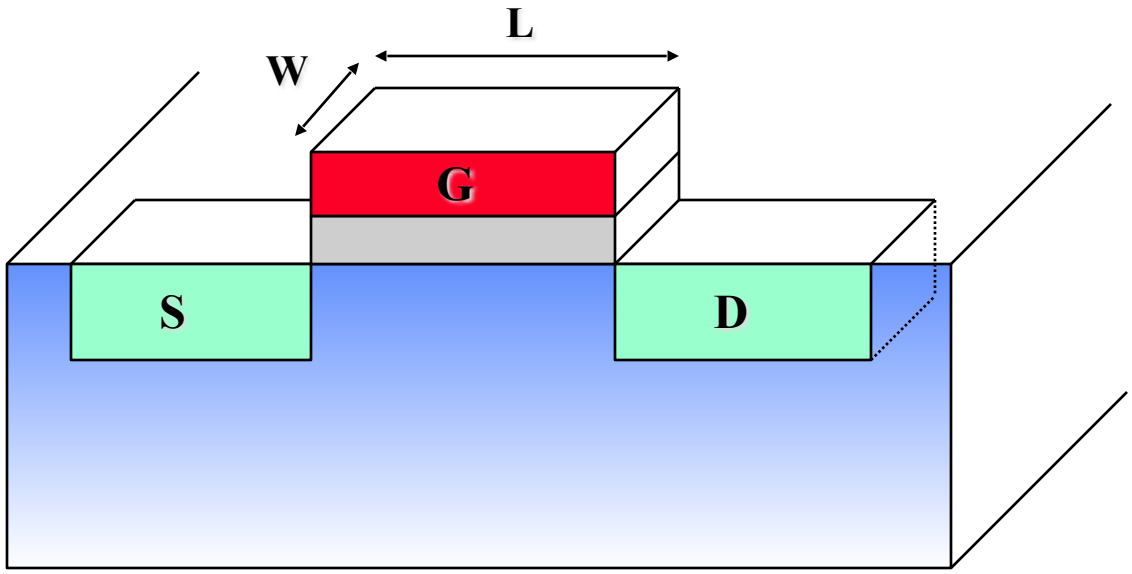
- consumo estático : antigamente ≈ 0
- consumo dinâmico (transição) = Iout + Icc
- consumo total = estático + dinâmico

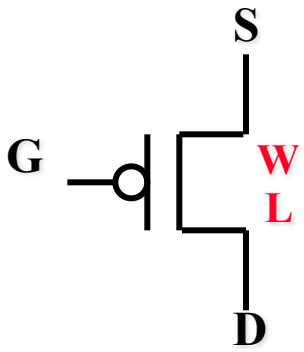



* A variação de W e L afeta o tempo de transição dos sinais e o consumo da porta lógica.

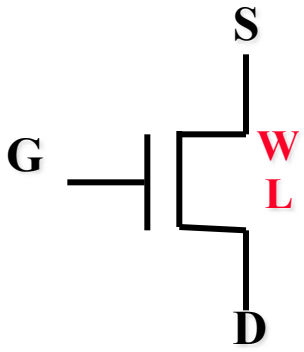
# Dimensionamento do Transistor MOS



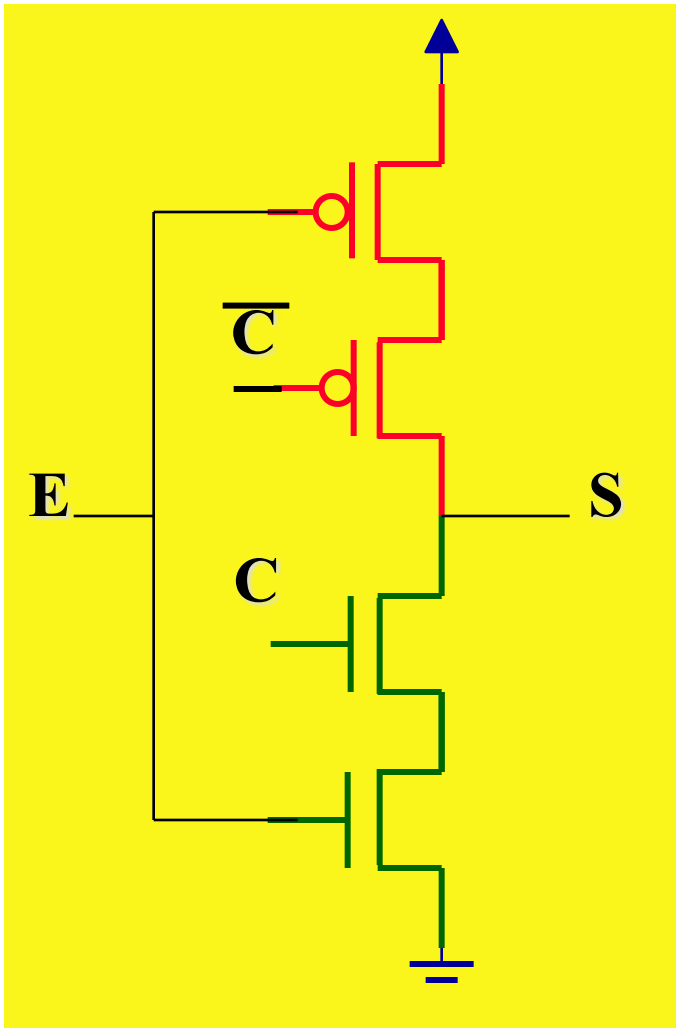

Análise de 'r' ('*on*') e C:

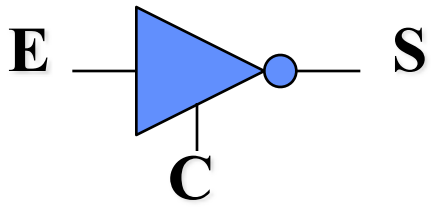
- W ↑ : r ↓ e C ↑
- L ↑ : r ↑ e C ↑



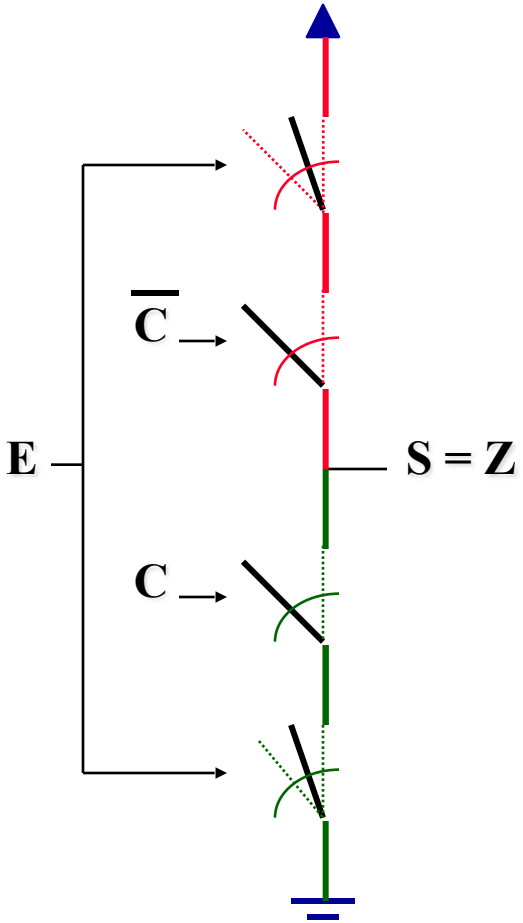
# Alta Impedância (Z)

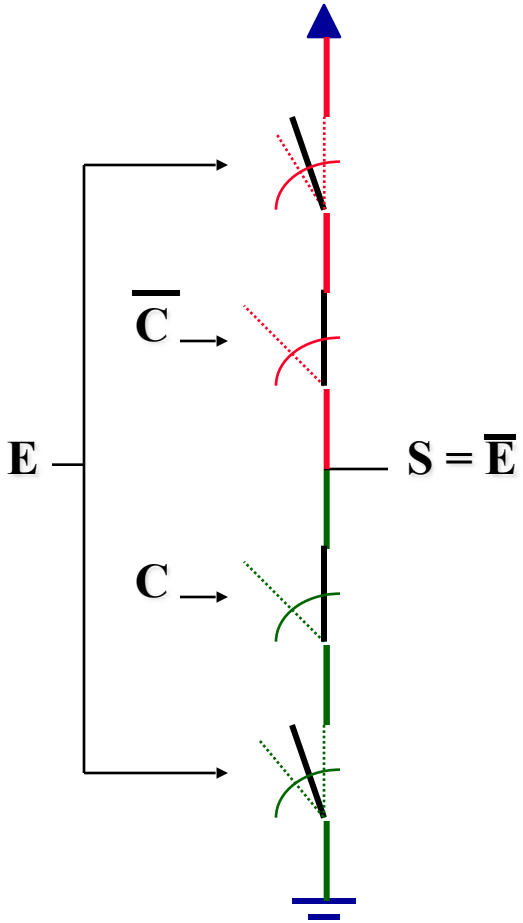
## Inversor Tri-State (INVTR)



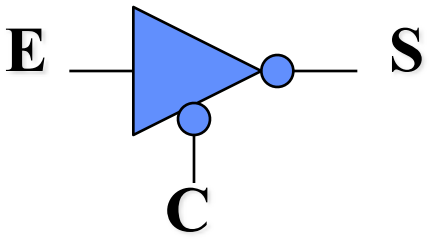




| E | C | $\overline{C}$ | S |
|---|---|---|---|
| 0 | 0 | 1 | Z |
| 1 | 0 | 1 | Z |
| 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 |



## Outra opção... (*controle negado*)

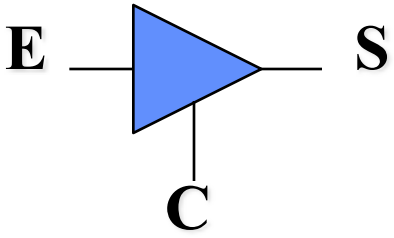



| E | C | S |
|---|---|---|
| 0 | 0 | 1 |
| 1 | 0 | 0 |
| 0 | 1 | Z |
| 1 | 1 | Z |

*OU*

| C | S |
|---|---|
| 0 | ~~E~~ |
| 1 | Z |

## Buffer Tri-State (BUFTR)

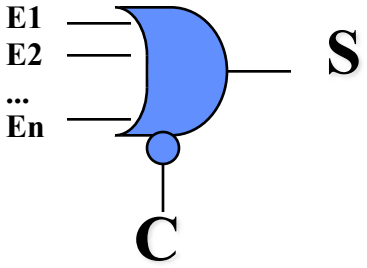


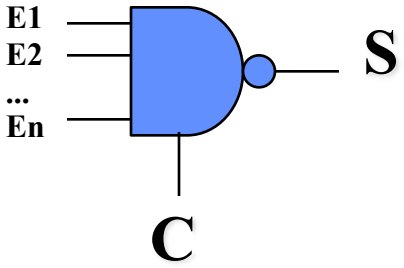

| E | C | S |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | Z |
| 1 | 1 | Z |

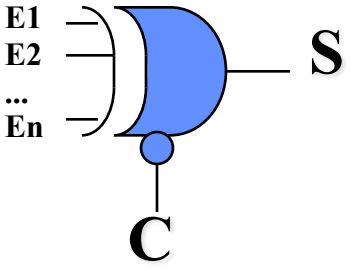
*OU*

| C | S |
|---|---|
| 0 | Z |
| 1 | E |

*** PODE-SE PENSAR EM QUALQUER PORTA LÓGICA COM SAÍDA TRI-STATE OU ALTA-IMPEDÂNCIA (Z) !!!**

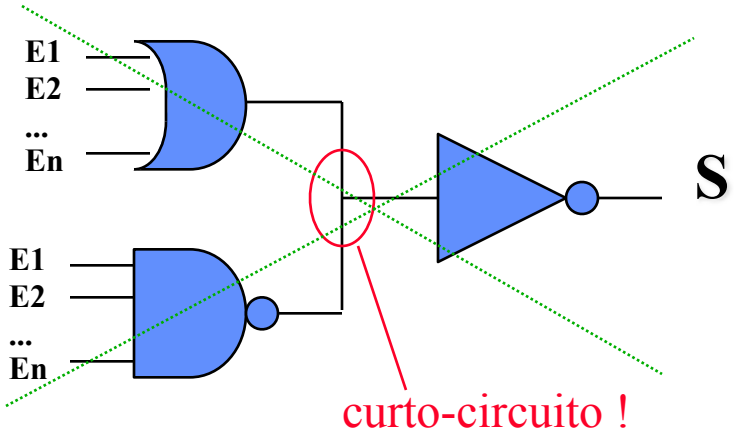


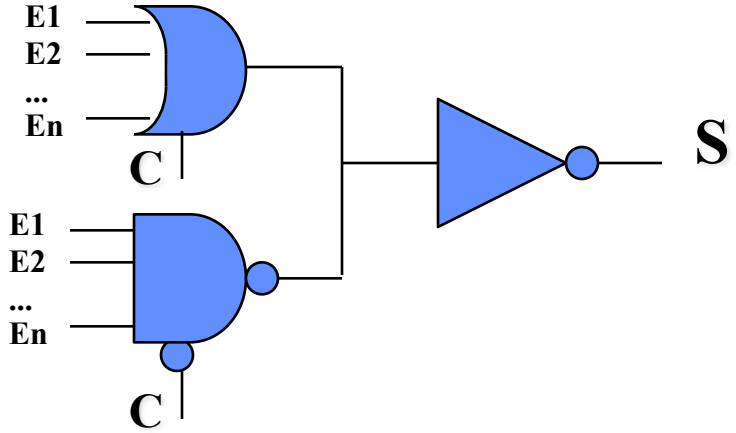



# Uso de Porta Tri-State ...

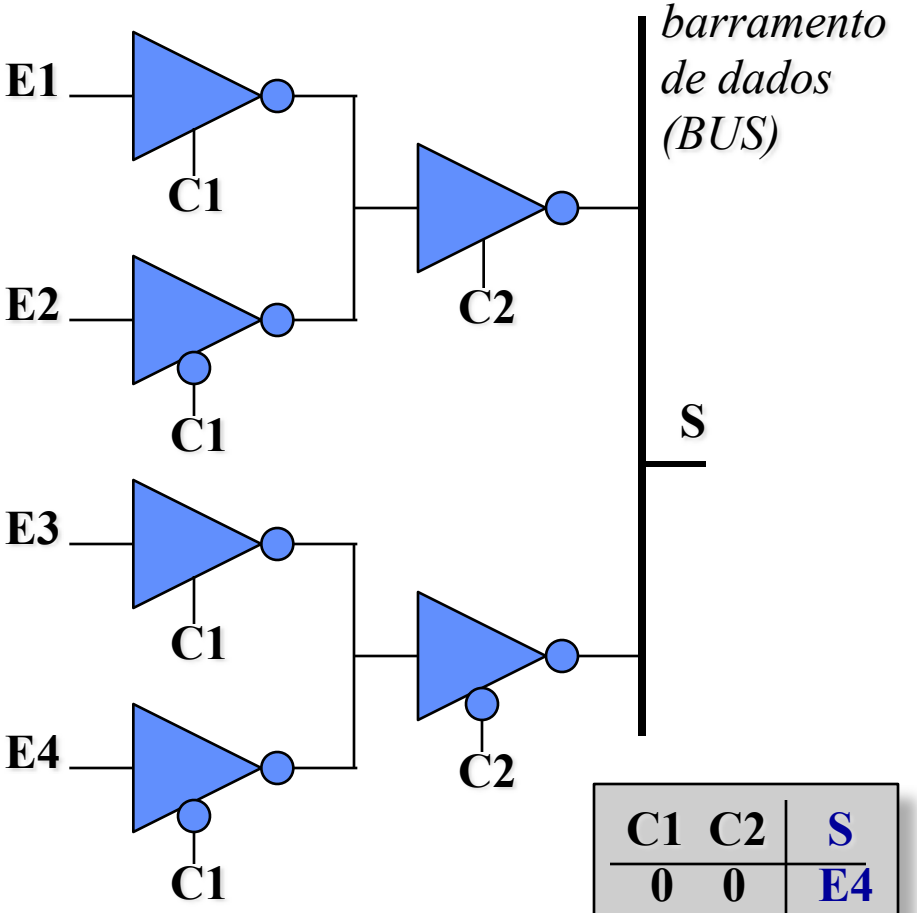
* NÃO É PERMITIDO EM CMOS :




* CORRETO :




* BARRAMENTO DE SINAIS :




| C1 | C2 | S |
|---|---|---|
| 0 | 0 | E4 |
| 1 | 0 | E3 |
| 0 | 1 | E2 |
| 1 | 1 | E1 |