Arquitetura e Projeto VLSI I

UFRGS – PPGC - 2003

Parte de Projeto - Marcelo Johann

AULA 2

Referências básicas sobre microeletrônica

http://vlsi.wpi.edu/webcourse/toc.html

Chapters 2 and 3- Process and layout

Reis, R. A. L. Concepção de Circuitos Integrados,

Capitulos 3 e 4: processo e portas lógicas

Carro, L., Projeto e Prototipação de Sistemas Digitais

Capítulo 2 até 2.3: introdução a VHDL

O que é VHDL?

VHSIC Hardware Description Language

Very High Speed Integrated Circuit program

DoD – Department of Defense – década de 80

- tempo de projeto muito longo (até 6 anos)
- alto custo de manutenção
- dificuldade de comunicação entre fabricantes

Objetivo principal: descrição/simulação

- Primeira versão 1985
- IEEE 1076-1987
- IEEE 1076-1993

Descrições de Projeto

Why use a HDL (Hardware Descriptive Language) ?

http://eleceng.ucd.ie/~rreilly/Digital/HDL-Design%20Issues.pdf

Situação de VHDL hoje:

Padrão aceito por CAD tools e projetistas

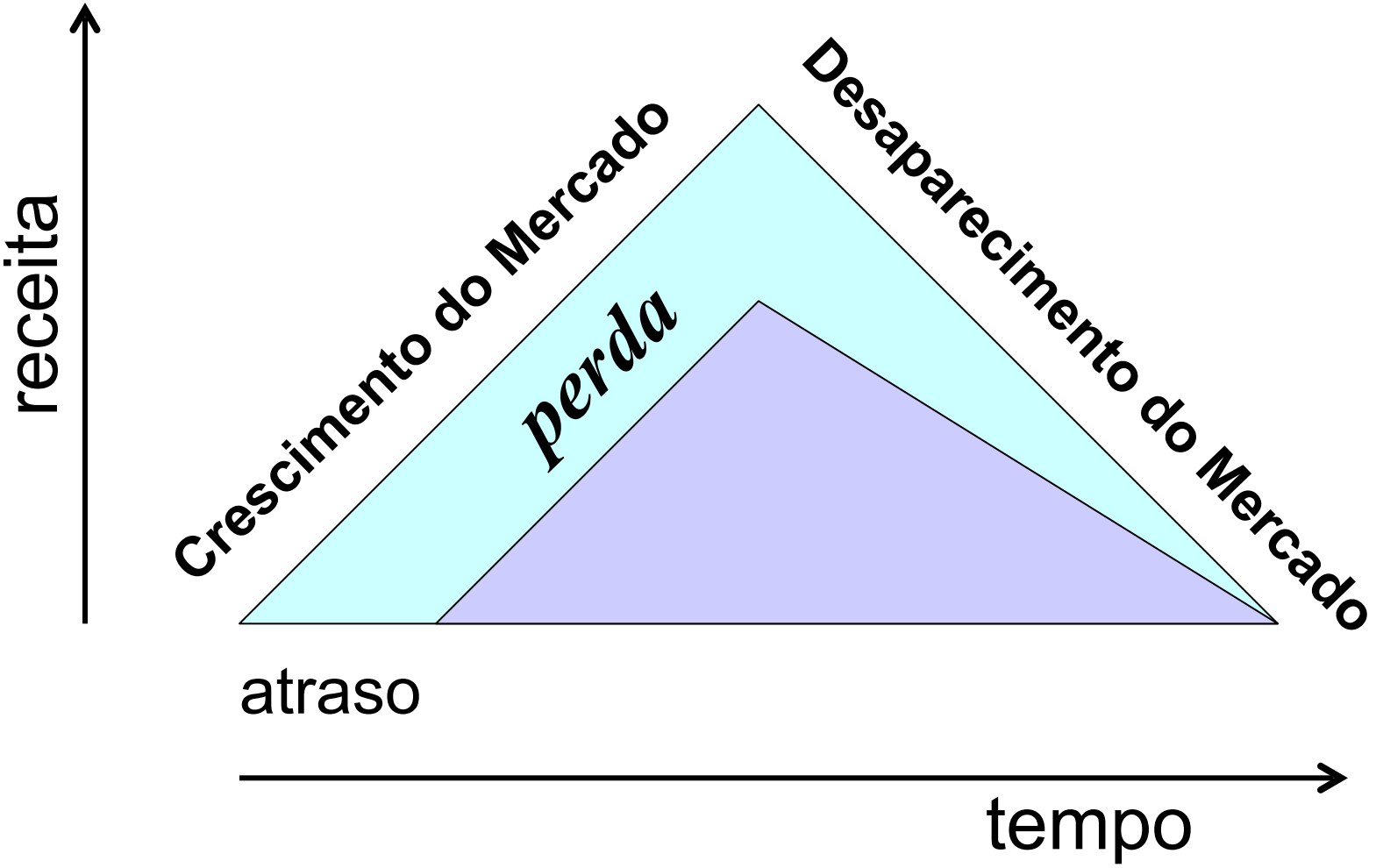
Síntese: inferência de Hardware

IEEE 1164 standard package

Concorrente: **Verilog** – E.U.A.

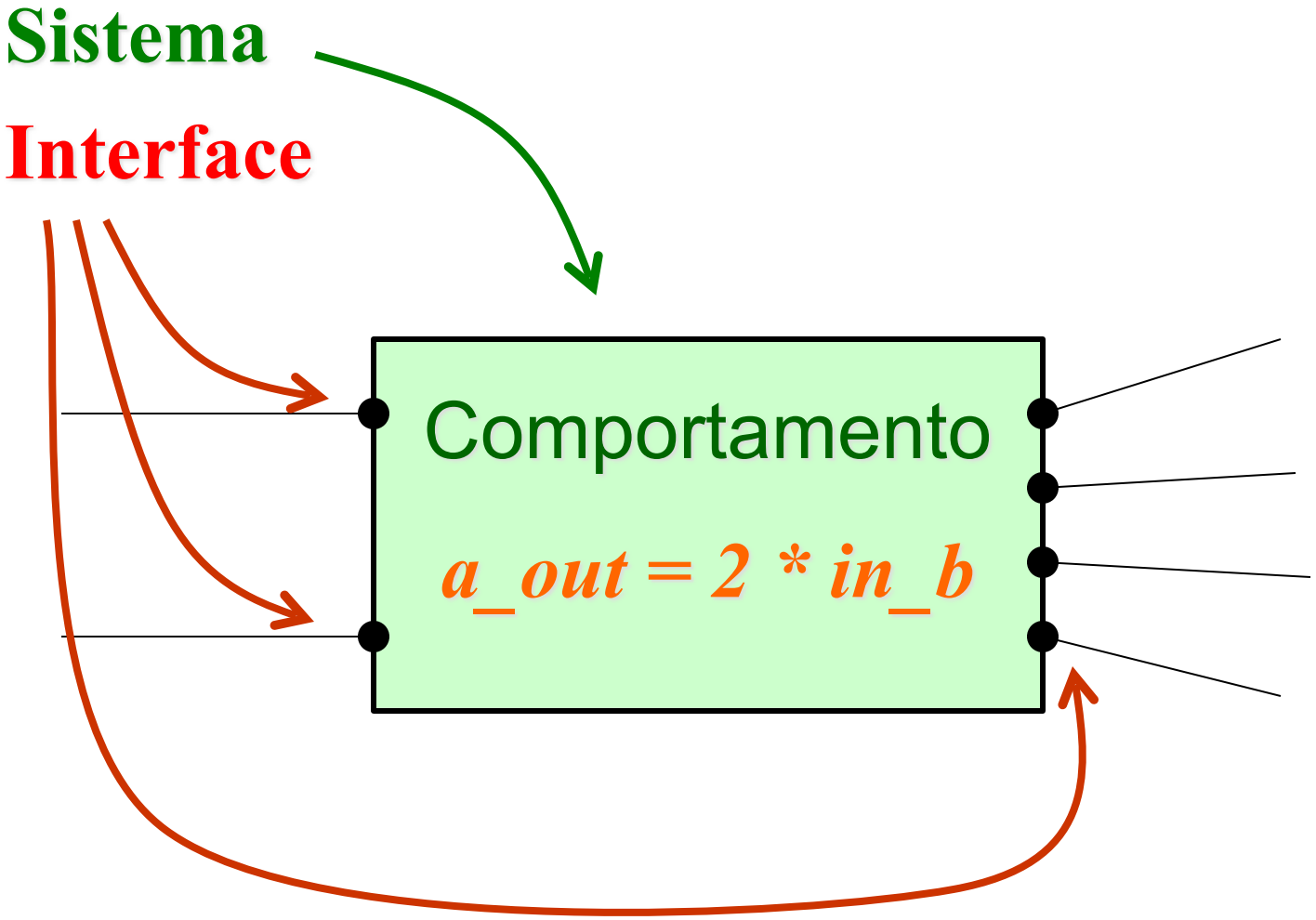
Mercado

10%-20% design → 70%-80% final cost
5%-10% time formulating requirements



Elementos de Hardware

SW é seqüencial, HW é concorrente:



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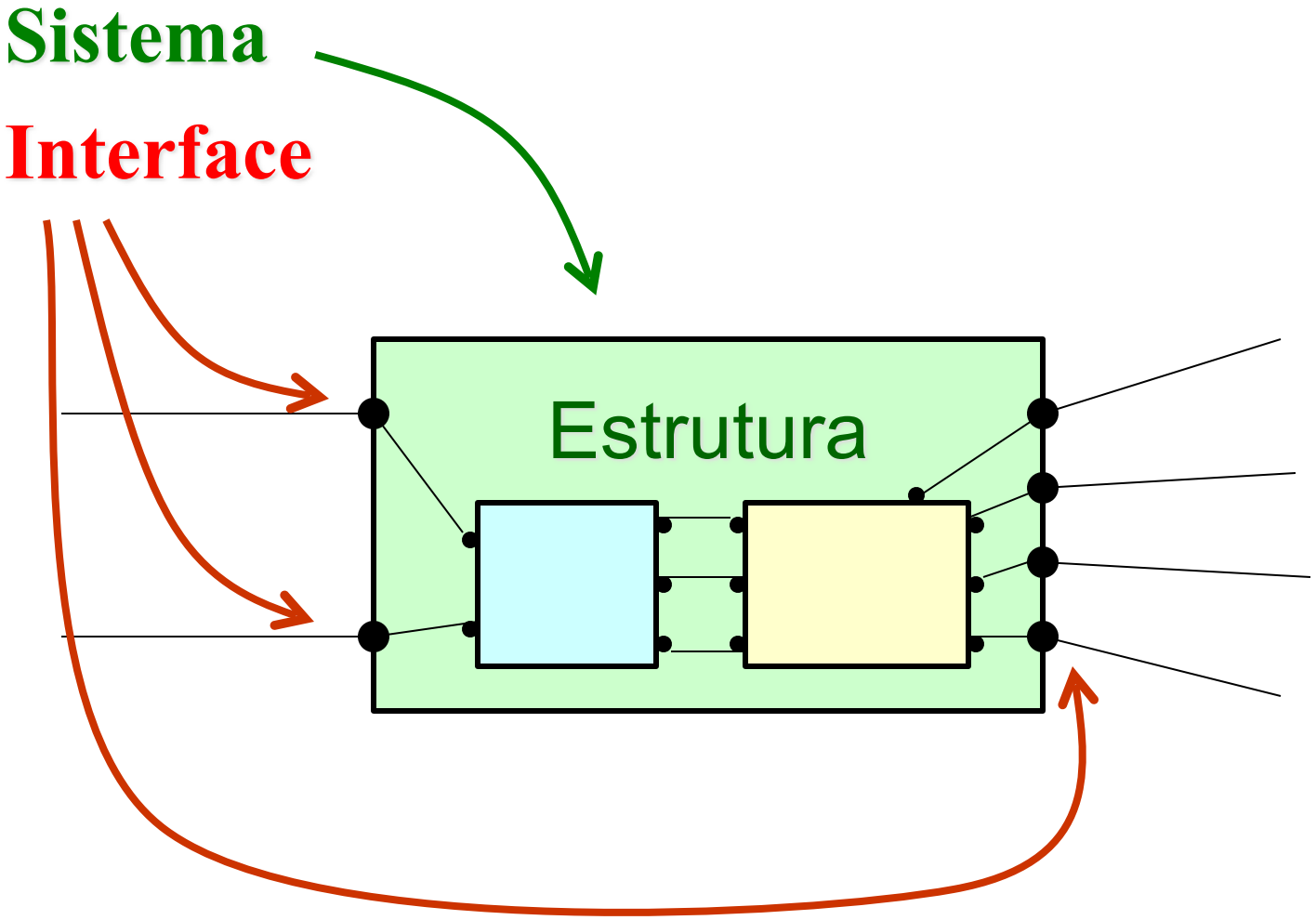
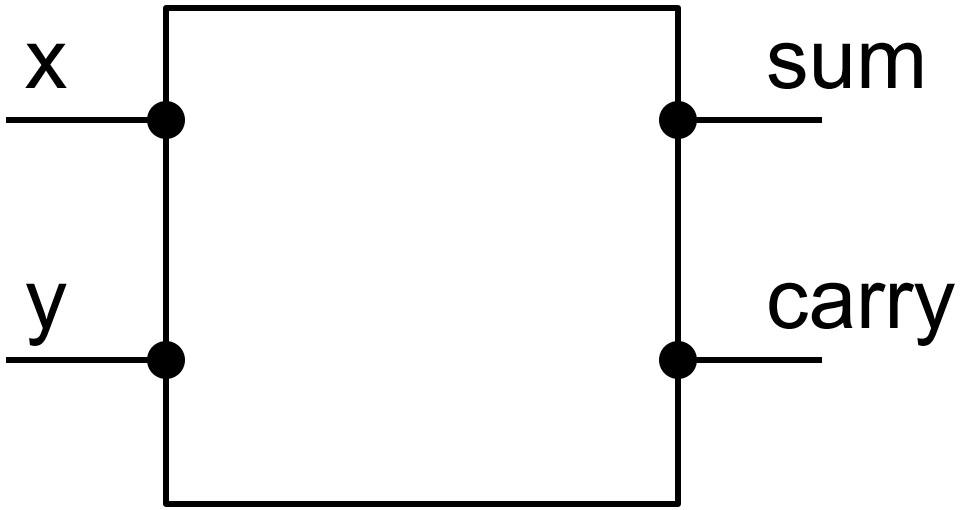


Entidade e Interface em VHDL

```
entity half_adder is
port ( x, y: in std_ulogic;
       sum, carry: out std_ulogic );
end entity half_adder;
```

IEEE 1164

1993



Sinais e Valores IEEE 1164

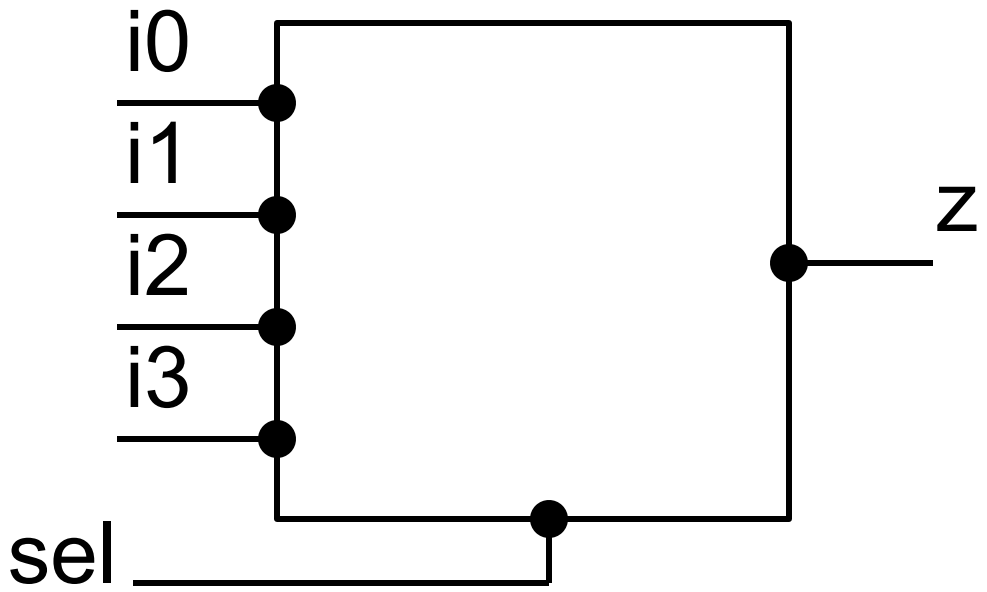
std_ulogic

std_ulogic_vector

Value	Interpretation
U	Uninitialized
X	Forcing Unknown
0	Forcing 0
1	Forcing 1
Z	High Impedance
W	Weak unknown
L	Weak 0
H	Weak 1
-	Don´t care

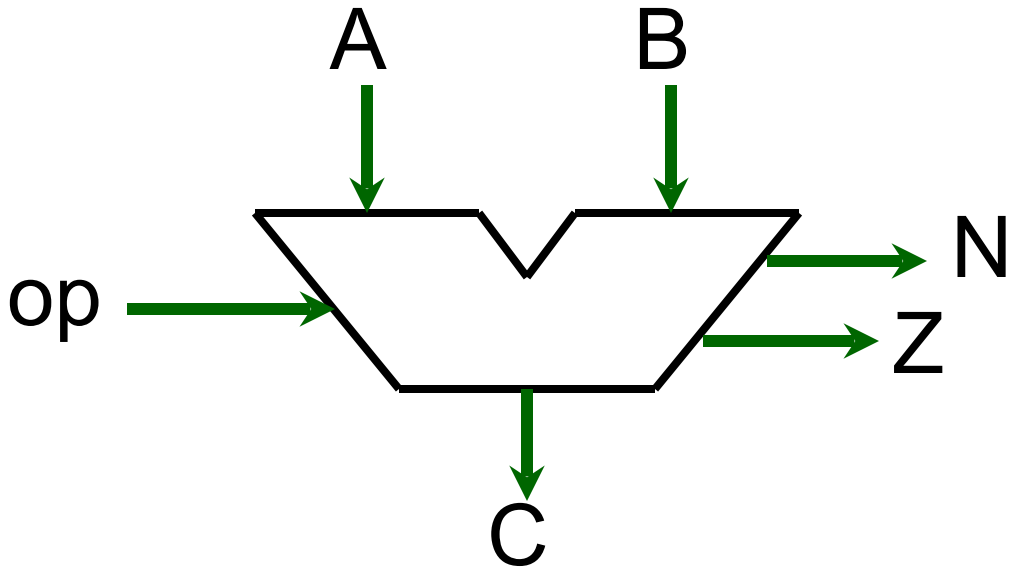
Multiplexador 4 para 1

```
entity mux is
port ( i0, i1 : in std_ulogic_vector (7 downto 0);
       i2, i3 : in std_ulogic_vector (7 downto 0);
       sel    : in std_ulogic_vector (1 downto 0);
       z      : out std_ulogic_vector (7 downto
0)     );
end entity mux;
```



ULA de 32 bits

```
entity ula32 is
port ( A,B : in std_ulogic_vector (31 downto 0);
       C   : out std_ulogic_vector (31 downto 0);
       op  : in std_ulogic_vector (5 downto 0);
       N,Z : out std_ulogic );
end entity ula32;
```



Arquitetura em VHDL

```
architecture behavior of half_adder is
-- declarations go here
begin
-- place description of behavior here
end architecture behavior;
```

1993

Concurrent Signal Assignment statements

```
architecture behavior of half_adder is
begin
sum <= ( x xor y) after 5 ns;
carry <= ( x and y) after 5 ns;
end architecture behavior;
```

x	y	sum	carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Concurrent Signal Assignment statements

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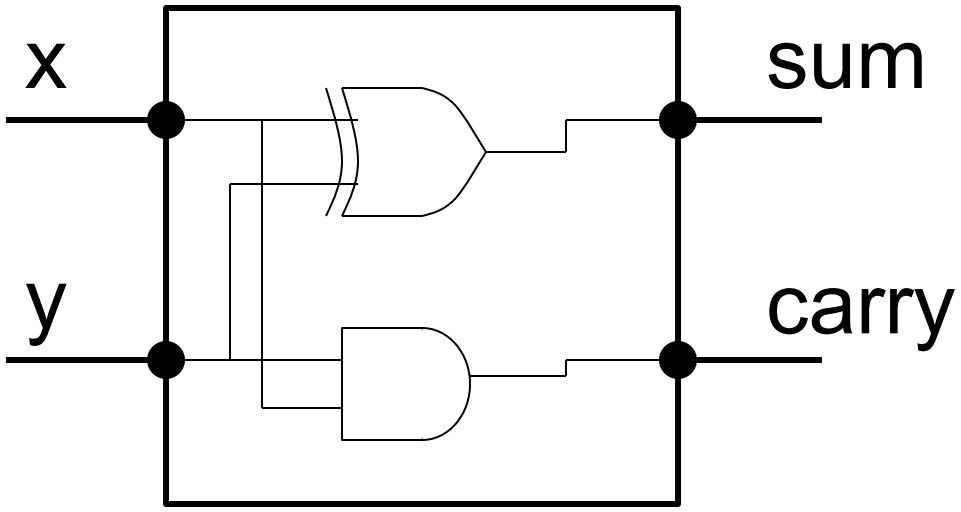

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