Arquitetura e Projeto VLSI I

UFRGS – PPGC - 2003

Parte de Projeto - Marcelo Johann

AULA 4

Conteúdo da Aula

Usando MAX+PLUS II da Altera

Simulação comportamental: Processos

- sequential statements
- assinalamento a sinais externos
- execução em tempo 0
- sensitivity list
- construções
- inicialização: todos executam 1 vez
- signal versus variable
- construções wait

Exemplo de memória pequena

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
entity mem8 is
port ( address : in unsigned (31 downto 0);
        wrdata: in std_logic_vector (31 downto 0);
        memwrite, memread: in std_logic;
        rdata : out std_logic_vector (31 downto 0)
        );
end entity mem8;
```

Exemplo de memória pequena

```
architecture behavior of mem8 is
    type memarray is array(0 to 7) of
        std_logic_vector (31 downto 0);
begin
memproc : process (address,wrdata) is

    variable datamem : memarray :=
    X“00000000”, X“00000000”,
    X“00000000”, X“00000000”,
    X“00000000”, X“00000000”,
    X“00000000”, X“00000000” );
    variable addr : integer ;
```

Exemplo de memória pequena

```
    begin
    L1:
    addr := conv_integer(address(2 downto 0));
    L2:
    if memwrite = ´1´ then
    L3: datamem(addr) := wrdata;
    elsif memread = ´1´ then
    rdata <= datamem(addr) after 10 ns;
    end if
    end process memproc;
end architecture behavior;
```

Exemplo de processos concorrentes

```
library IEEE;
use IEEE.std_logic_1164.all;

entity meiosoma is
port ( x,y : in std_logic ;
        sum, carry: out std_logic ;
        );
end entity meiosoma;
```

Exemplo de processos concorrentes

```
architecture behavior of meiosoma is
begin

sumproc : process (x,y) is
    begin
    if (x = y) then
        sum <= ´0´ after 5 ns;
    else
        sum <= (x or y) after 5 ns;
    end if;
    end process sumproc;
```

Exemplo de processos concorrentes

```
carryproc : process (x,y) is
    begin
    case x is
    when ´0´ =>
        carry <= x after 5 ns;
    when ´1´ =>
        carry <= y after 5 ns;
    when others =>
        carry <= ´X´ after 5 ns;
    end case;
    end process carryproc;

end architecture behavior ;
```

Exemplo de processos e CSA

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;

entity mem4 is
port ( address : in std_logic_vector (7 downto 0);
       wrdata: in std_logic_vector (7 downto 0);
       memwrite, memread: in std_logic;
       ck, reset: in std_logic;
       rdata : out std_logic_vector (7 downto 0)
       );
end entity mem4;
```

Exemplo de memória e CSA

```
architecture behavior of mem4 is
    signal dmem0,dmem1,dmem2,dmem3:
        std_logic_vector (7 downto 0);
begin
rdata <=    dmem0 when address(1 downto 0) = ´00´
                                  and memread = ´1´else
            dmem1 when address(1 downto 0) = ´01´
                                  and memread = ´1´else
            dmem2 when address(1 downto 0) = ´10´
                                  and memread = ´1´else
            dmem3 when address(1 downto 0) = ´11´
                                  and memread = ´1´else
            x“00”;
```

Exemplo de memória e CSA

```
writeproc : process (clk) is
    begin
    if (rising_edge(clk)) then
        if reset = ´1´then dmem0 <= x“00”;
            dmem1 <= x“11”; dmem2 <= x“22”; dmem3 <= x“33”;
        elsif memwrite = ´1´ then
            case address (1 downto 0) is
            when “00” => dmem0 <= wrdata;
            when “01” => dmem1 <= wrdata;
            when “10” => dmem2 <= wrdata;
            when “11” => dmem3 <= wrdata;
            when others  => dmem0 <= x“ff”;
            end case;
        end if; end if;
end process writeproc ;
end architecture behavior ;
```

Para próxima semana

Instalar Max+Plus II

Simular exemplos VHDL da aula