Layout Synthesis using Transparent Cells and FOTC Routing

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ABSTRACT

This paper describes an original methodology for random logic layout generation. A Full Over-the-Cell routing model is used to realize the connections over the transistors by using "transparent cells". It is presented a system under development that implements these concepts, called TRAMOII. A small circuit generated with a partial automation is used to compare the results of this methodology with Standard Cell and Linear-matrix layout styles.

I. Introduction

With the increase in VLSI circuits complexity, it is fundamental the use of improved EDA tools to carry out the design of such circuits. This automation cannot sacrifice the design performance or integration density, but the Standard Cells, the most widely used methodology for random logic generation, leads to a reasonable waste of area, performance, flexibility, and power dissipation, because of its topological structure, which is shown in fig. 1. This structure was introduced because of its simplicity, allowing the automatic generation of several kinds of circuits by using pre-designed cell libraries. However, the search for new styles and methodologies for layout synthesis, specially by using technology independent module generation, can be used to produce more efficient circuits.

To minimize the waste of area with the Standard Cell routing channels, several techniques were proposed, in which some connections are made over the cells using the layers not occupied. This is called Over-the-Cell Routing or OTC [4] [5] [2] [3]. An example of the physical model used for OTC routing is shown in fig. 2. It is important to note that in Standard Cells with 2 metal layers we do not need feedthroughs because the second metal layer can cross over the cell rows. But when using OTC routing, the first metal layer is required for cell design and the second one is required for the OTC connections. Thus, the feedthroughs are needed, and the reduction on the channel height will not be so good because it will impose the consumption of other resources (horizontal space).

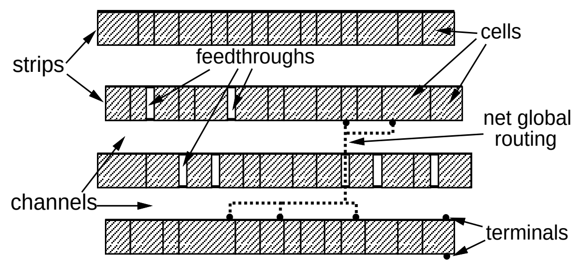

Figure 1: Standard Cells circuit structure.

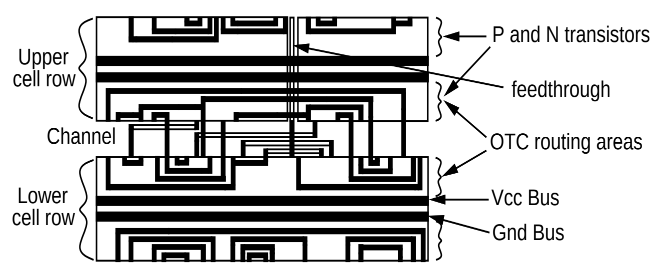

Figure 2: Physical model for OTC routing.

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The availability of more than two metal layers have also been studied in several ways to improve the OTC routing [8] [15], and new OTC models for routing and for cell design have been proposed [16] [1] [6]. In all this models, however, the circuit is normally divided into strips and channels, and these channels are only partially minimized by the use of a planar routing over the cells.

II. Transparent Cell Approach

The TRANsparent Cell Approach (TRANCA) [12] was proposed based on the observation of microprocessor layouts manually designed in the 70's. In the TRANCA original layout style, the connections are performed over the cell active areas, as shown in fig. 3, resulting in an appropriate combination between cell and routing structures, not using routing channels.

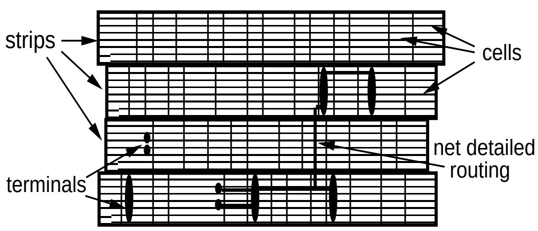

Figure 3: Transparent Cell circuit structure.

In this approach, the cells are specially designed to offer transparency for the routing, and their terminals are optimally positioned to provide, at the same time, easy external access and good intracell organization. A detailed transparency can be achieved by designing the cells with all metal elements oriented and aligned according to a virtual grid that represents the positions of horizontal and vertical routing tracks. Figure 4 shows a nand3 transparent cell where we can see these features.

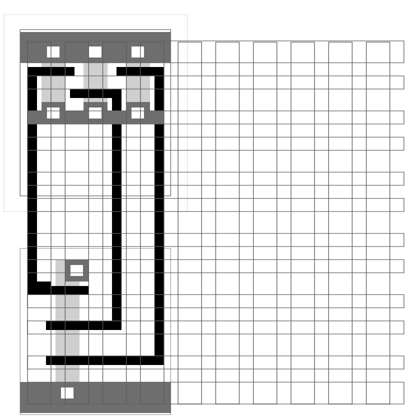

Figure 4: A nand3 transparent cell

The routing problem resulting from using the Transparent Cell Approach is defined as "Full Over-the-Cell" Routing model. The word "Full" means that it maximizes the overlapping of the routing over the cell layouts. A symbolic routing can be made using the virtual grid over the cells according to restrictions extracted from cell layouts.

The FOTC routing greatly differs from the previous OTC models. It is not naturally divided into well defined sub problems, as it was the Standard Cell routing with or without OTC improvements. Figure 5 shows the position of a connection between two neighboring cells in a Standard Cell approach without OTC, in a Standard Cell with OTC routing, and in the TRANCA FOTC routing model. By using transparency, the interstrip connections are also much less expensive, because they do not need feedthroughs allocation as it is required for the OTC routing.

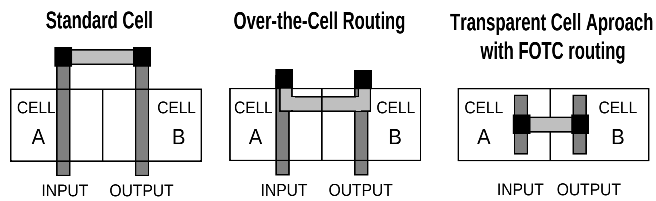

Figure 5: Connections between neighbouring cells.

III. The TRAMOII synthesis system

TramoII [13] is a layout synthesis system under development at UFRGS, addressing random logic generation as an alternative to Standard Cells. In this system, TRANCA concepts are optimized considering a performance driven result. The research work related to TramoII is centered in three main topics: dedicated partitioning/placement, routing, and cell generation. The FOTC routing is done by an apropriate environment already developed, called MARTE (MAtrix RouTing Environment) [9].

A. TramoII system structure

The first version of TRAMOII will perform circuit synthesis based on the use of cell libraries. However, its advanced features will include symbolic cell generation with variable strip heights. Figure 6 shows the overall flowchart of the TramoII system with these advanced features.

Initially, the circuit description is decomposed, taking into account the target resources, resulting in a flat netlist composed of leaf cells. The intracell structure is passed to symbolic cell generation, while the circuit structure (interconnection of leaf cells) is used in the placement of the whole circuit, with some cell symbolic information. It includes minimum and maximum number of vertical and horizontal tracks that can be used to generate each cell.

After the placement step, symbolic cells are expanded, considering the resulting strip heights. This fact has been already considered in the placement step. This expansion from symbolic representation is carried out by compacting the cell layouts, but it must consider the constrains imposed by the TRANCA grid organization. These constraints are present in the metal elements and in the cell terminals, which will be accessed by connections in the metal layers.

From cell layouts it is extracted the symbolic abstraction used for routing. This abstraction includes the routing restriction matrix and the terminals description. After the detailed routing, the corresponding layout is added to the cell layout descriptions to complete the description of the final circuit masks.

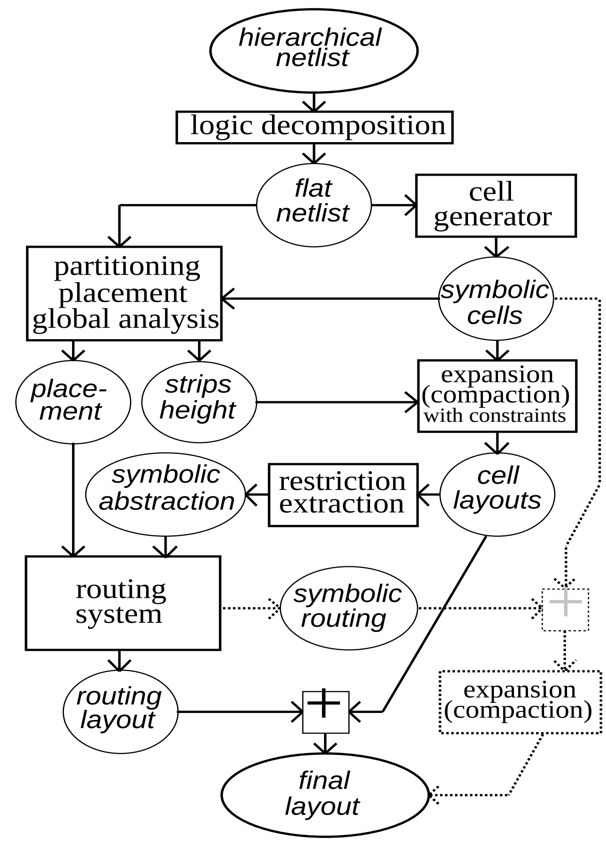

Figure 6: TramoII System Structure.

Since the cells and the routing are symbolically generated, it is also possible to refuse the pre-expanded cell layouts and to join the symbolic cells and symbolic routing descriptions to make a global expansion (with compaction). This option is shown with dashed lines, and it could be useful to make the symbolic routing over real cell layouts, but using an optimized compaction with the knowledge about exact terminal connections.

B. Automatic generation of transparent cells

An important feature of TramoII system is the automatic cell generation. The main "impact" of this approach is to eliminate the need of updating a limited cell library every time the technology changes. A goal when generating the cells is to obtain transistor dispositions that fit well in the FOTC routing grid. The transparent cell generation uses some basic gate configurations and an algorithm for composing any possible CMOS complementary logic function. So, it is possible to generate complex gates with good transparency and transistor density. With apropriate technology mapping, the use of "aois" can reduce the total amount of transistors in a circuit in about 30% to 40%, reducing also delay and power consumption.

IV. Practical Results

In order to evaluate the results produced by the system, a 4-bit arithmetic and logic unit (ALU181) was generated by using a partial automation. It was used an adapted placement and the FOTC routing was performed by Marte system. The cells were manually designed according to the transparent cell automatic generation guidelines.

The resulting circuit, called Alu80, was compared to one generated with Cadence Edge 2.1 Standard Cell (called SC1), and it was also compared to two other circuits synthesized by TROPIC linear-matrix generator ([11]), a system developed in cooperation between UFRGS and LIRMM, Monpellier, France. The first TROPIC circuit has all transistors with Wp=Wn=8 micra (Trpw=8), and the second one has the same transistor sizes as the TramoII cell library (Trpw=T2). Table 1 summarizes the results of this comparison (see [10]), showing final area, average of transistor sizes, integration density, delay in the critical path, power consumption during the simulation time, and parasitic capacitances extracted from the layouts.

Circuit	area mm2	ave. w	tran/ mm2	tdlh ns	pow mW	cap. sum
SC1	.1499	13.5	3028	11.5	-	-
Trpw=8	.1350	8.0	3140	15.6	3.9	10.01
Trpw=T2	.1298	3.5	3250	21.1	3.1	9.38
Alu80	.1225	3.5	3444	18.8	2.81	7.72

Table 1: Information about implemented circuits.

The circuits present different electrical performance according to the different transistor sizes they have. However, it is possible to verify that the module generation alternatives can produce interesting performance/cost ratios if compared to the traditional standard cell methodology. The TramoII layout seems to have the best efficience. It is faster than the linear-matrix version with the same transistor sizing and presents less power consumption.

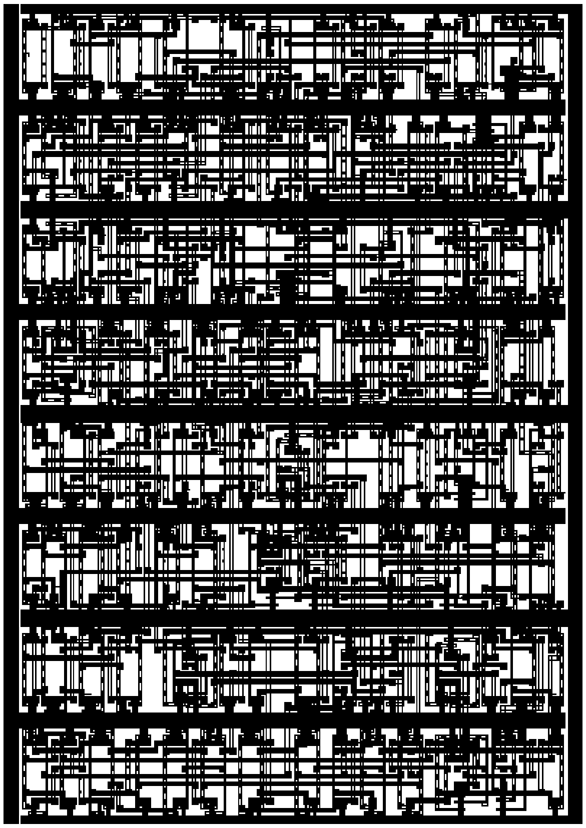

Figure 7: TramoII layout of the Alu181 circuit.

V. Conclusion

The Transparent Cell Approach with Full Over-the-Cell routing can be used as an alternative to traditional Standard Cells, providing layout flexibility and good global/local optimization. It alows the implementation of really custom circuits considering specific design constraints, performance driven designs and low power. Prediffused approaches can also be optimized by using FOTC routing (sea-of-gates or sea-of-cells [7]), because in this model it is not necessary to use routing channels or to waste transistor rows to make the routing, as it is usually done.

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