A Comparison between Random Logic Layout Design Methodologies

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ABSTRACT

This paper presents an experiment about the random logic generation employing non-conventional layout styles. It was implemented a known combinational circuit by using different layout design methodologies in order to evaluate the results produced in each case. The methodologies considered are: Standard Cell; Linear-matrix style of the TROPIC module generator; and the Full Over-the-Cell Routing model according to the TRAMOII module generator (under development).

The possible comparisons are presented, and the main differences, advantages and disadvantages of each approach are discussed based on the practical results. Several performance aspects are covered, such as integration density, delay, power consumption, as well as the concepts involved with the models.

1 Introduction

The Standard Cell is the most widely used layout methodology for random logic generation. This technology was introduced because of its simplicity, allowing the automatic generation of several kinds of circuits by using pre-designed cell libraries. Despite all the advantages and the improvements, the structure of this approach leads to a reasonable waste of area, performance, flexibility and power dissipation, due to its fixed topological disposition and the cell library limitations. Manually designed circuits usually present a better performance/cost ratio by using different layout structures.

1.1 Module generation alternatives

The module generation is an alternative in which specific layout structures are completely generated from logic descriptions. Dedicated structures are normally used to easily implement some kinds of circuits, such as datapaths, or PLAs. Moreover, random logic layout generation can also be used to improve the layout quality as an alternative to Standard Cell designs. In this case, the CAD system must be more complex, ensuring the layout correctness and the required electrical performance. The advantages are: technology independence, unrestricted cell generation (not limitted by the cell libraries), and specific matching with the design constraints. The use of such systems, for example like gate-matrix or linear-matrix layout styles, is not yet diffused in comercial designs mainly because of its complexity and availability.

1.2 Transparent Cell Approach

The Transparent Cell Approach [REI 87] [REI 88] was proposed based on observations about manually designed microprocessor layouts of the 70's. The main goal is to achieve an automatic generation of random logic by using a layout structure with the same characteristics and advantages of the manually designed ones. In this original style, the connections are routed over the cells active area, as shown in figure 1. The cells are specially designed to offer transparency for the routing layers.

The routing model used in this approach is defined as "Full Over-the-Cell" routing (FOTC) [JOH 94b] and it greatly differs from the well-studied Over-the-Cell Routing models (OTC), which are usually channel routing improvements in the traditional Standard Cell circuit structure ([SHE 93]).

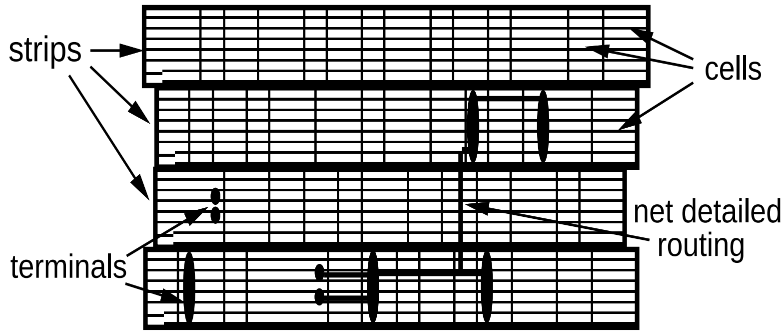

Figure 1: Transparent Cell circuit structure.

1.3 Full Over-the-Cell Routing

Figure 2 shows the position of a connection between two neighboring cells in a Standard Cell circuit, in a Standard Cell with OTC routing, and in the TRANCA FOTC routing model. Of course, in the last case, the cells are not so small (for the same transistor sizing), but the position of the connections and the cell elements are optimized together. By using transparency, the interstrip connections are also much less expensive, because they do not need feedthroughs.

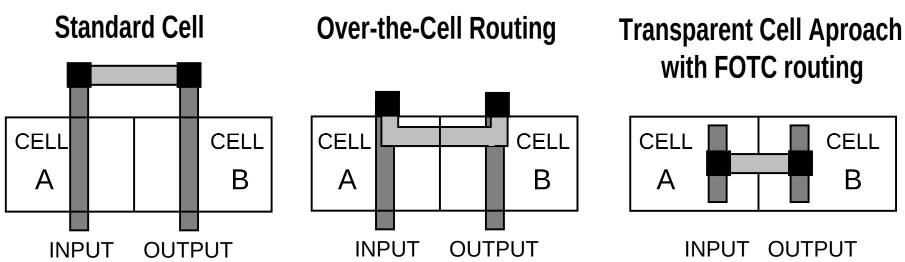

Figure 2: Connections between neighboring cells.

2 CAD tools used

In this paper, we present a comparison between the described methodologies for automatic layout generation based on the practical results produced by the implementation of a small circuit in the appropriate environments. The following subsections describe the CAD environments used in this experiment.

2.1 Cadence Edge Standard Cell

The Standard Cell version was generated by using the **Cadence Edge 2.1** environment, with the **ES2** 1,2um cell library. The CAD system has a schematic entry and functional simulation facilities. It generates the final layout of the entire circuit (with PADs) by including the cells of the proprietary library.

2.2 TROPIC linear-matrix

Linear-matrix versions were implemented by using the TROPIC module generator [MOR 93] [MOR 94], developed in the scope of a cooperation project between UFRGS/Porto Alegre and LIRMM/Montpellier(France). The system is partially integrated within **Cadence Edge** and **Opus** environments to provide compaction, layout view and other facilities. It can generate circuit blocks of any size (limited by the compactor), from a spice netlist description, for 2 metal layer technologies.

2.3 TRAMOII Full Over-the-Cell Routing

The TRANCA FOTC circuit version was generated according to TRAMOII system [REI 93] [JOH 94b]. This CAD system is composed by a set of independent tools and dedicated research works, and it is not yet finished. The research is centered in the FOTC routing, dedicated placement and automatic transparent cell generation. The FOTC routing is done by MARTE routing system [JOH 93] [JOH 94a], but current version of TRAMOII uses manually designed cell libraries and have neither dedicated placement nor cell generation implementations finished.

3 Theoretical differences and considerations

TROPIC system explores technology independence by using a linear-matrix layout style, but it performs only a partially effective transparency (only in metal 2). TRAMOII system explores mainly the transparency concept in both metal layers, but to be technology independent the implementation of an automatic transparent cell generator must be finished.

Another main difference between these two systems concerns the way the routing is done. In TROPIC, all layout elements are symbolically generated according to the needs. Then, the symbolic description is translated to the real layout through a compaction step. However, in TRAMOII, the symbolic routing is done over an already established layout (over the cell layouts), being adapted to it instead of influencing it (generating the needed space or tracks, for example).

The advantage of TROPIC model is that the needed area is always allocated, while in TRAMOII there is a necessity of a good area estimation during the placement and during the cell generation phases to allow a complete routing, since there are no facilities to include spaces in the routing step. The advantage of TRAMOII style is that the generated routing presents the maximum overlapping with the cells, and also the inexistence of the circuit compaction (there is only cell restricted compaction) imposes no constraint on the circuit size.

4 Implemented circuits

The circuit used in the comparison is the ALU181, a 4-bit arithmetic and logic unit. The logic of the standard cell version was adapted according to the **ES2** cell library limitations, not thinking on the best or worst cases, but in a simple manner as any designer would do. The circuit implemented in TROPIC and in TRAMOII systems has the same logic, and it was taken from an adapted spice netlist. This netlist differs from the Standard Cell version in several ways: cell decomposition, negative logic mapping, and XOR implementation. There are advantages and disadvantages of these circuit versions when implemented in each environment. Thus, it will be assumed that this is a normal (practical) case of technology mapping done for different target layout styles, using different CAD systems.

The standard cell circuit will be called SC1. Two circuits were implemented using the TROPIC generator. The first, called Trpw=8, uses all transistors with wp=wn=8um. This large transistor sizes enforces the velocity and its use is similar to the SC approach. The second TROPIC version, the Trpw=T2, uses the same transistor sizes as the TRAMOII version, which were extracted from the layouts of TRAMOII cell library used.

TRAMOII version, called Alu80, was made with a partial automation. It was used the placement step from the old TRAMO prototype [LUB 90], adapted according to the TRAMOII cells (with different sizes). The remaining spaces, resulting from different strip lengths, have been distributed in the middle of the circuit at the points of maximum routing density. The TRAMOII basic cell library was manually designed according to the automatic transparent cell generation guidelines, [REI 93]. The restriction matrices were automatically extracted for MARTE FOTC routing.

5 Simulation and observed data

Trpw=8, Trpw=T2 and Alu80 circuits were fed into de **Opus** and **Edge** environments for DRC and logical extraction. The comparison between the extracted netlists was done by **Alliance** formal proof, resulting Ok. Figures 3 and 4 show the layouts of the implemented circuits: the Alu79 is an intermediate TRAMOII version. It has the same area and routing and differs from the Alu80 only by the cell library used, with smaller parasitic capacitances resulting from some adjustments;

All circuits were simulated in order to compare the delay in the critical path, observed in the output signal equal. The inputs were excited by input buffers and the output capacitance load used was 350fF (an empirical estimation). The SC1 circuit was simulated with the **Silos2** functional simulator taking into account the parasitic capacitances extracted after the detailed routing. The capacitance sum presented in table 1 for the circuit SC1 (marked with '*') is not the extracted one, but is the sum of the cell "total capacitance", presented in the cell library documentation. Trpw=8, Trpw=T2 and Alu80 circuits were simulated with the **Hspice** electrical simulator taking into account the extracted cell and routing capacitances (without extracting the resistences).

6 Results and comparisons

The following table shows the results for each implemented circuit. The observed data include size, number of transistors, average of transistor sizes (w), integration density, delay in the critical path, power consumption during the simulation time, and sum of extracted parasitic capacitances.

Circuit	x um	y um	area mm2	num. tran.	ave. w	tran. /mm2	tlh ns	thl ns	pow mW	cap. sum
SC1	530	283	.1499	454	13.5	3028	11.5	8.6	-	*22.18
Trpw=8	371	364	.1350	424	8.0	3140	15.6	6.0	3.9	10.01
Trpw=T2	319	407	.1298	422	3.5	3250	21.1	12.3	3.1	9.38
Alu79	296	414	.1225	422	3.5	3444	19.2	11.3	2.9	8.09
Alu80	296	414	.1225	422	3.5	3444	18.8	11.1	2.81	7.72

Table 1: Circuit informations and simulation with Cl=350fF

Taking into account the rise time of the equal signal (according to the critical path), the following statements are derived:

- SC1 circuit is 36% faster than Trpw=8 and it is 63% faster than Alu80.
- Alu80 circuit is 17% slower than Trpw=8 and it is 12% faster than Trpw=T2;
- Trpw=8 circuit is 35% faster than Trpw=T2 but it is only 4% greater;
- to be faster than Trpw=T2, Trpw=8 dissipates more power, while Alu80 circuit is faster than the same circuit but dissipates less power.
- TRAMOII circuit (Alu80) presents a smaller parasitic capacitances sum;
- TRAMOII circuit (Alu80) is 5.6% smaller than Trpw=8 and it is about 10% smaller than Trpw=T2;
- the size of Trpw=8 circuit is 90% of the SC1 size, and the size of Alu80 circuit is only 82% of the SC1 size, but considering the different number of transistors in the implementations the average of integration density achieved by the TRAMOII and TROPIC in these circuits is about 108% of the integration density obtained with **Edge** Standard Cell.

The implemented Standard Cell circuit is faster than TRAMOII and TROPIC ones, but it uses very large transistor sizes and it presents a resulting integration density that is a little bit smaller than the achieved by TRAMOII and TROPIC. Thus, it seems to be true that TROPIC and TRAMOII systems, and, generalizing, the module generation methodologies, can produce efficient layout structures when compared to the standard cell approach using mannualy designed cells. The automatic generation will take advantage by using appropriated transistor sizing, considering cell fanouts and also considering the critical path analysis. In these styles it is possible to generate complex gates (ANDORIs), reducing the number of transistors and the final layout area in about 30% to 40%.

6.1 Comparison between TRAMOII and TROPIC systems

With this experiment, and considering all related aspects, it is possible to make some specific conclusions about the presented alternative systems, that will be divided into: conclusions about the circuits of this experiment, conclusions about the CAD system implementations, and conclusions based on conceptual aspects.

Based on this experiment it is possible to say that a TROPIC circuit is slower than a TRAMOII circuit with the same transistor sizes. We have no comparison considering

TRAMOII with w=8, but taking into account that Trpw=8 circuit is faster than Trpw=T2 but it is bigger and it dissipates more power, while Alu80 circuit is also faster but it is smaller and it presents less power consumption, it seems to be clear that the performance/cost ratio in TRAMOII layout is better than in TROPIC layouts.

TROPIC implementation is complete and it can generate circuits with any transistor sizes on several technologies. TRAMOII is under development and does not have a set of basic tools for automatic generation yet, depending on a cell library. The algorithms used in TROPIC can also be enhanced to improve the results.

From the conceptual point of view, both systems present good ideas, but TROPIC layout style generates more parasitic capacitances, and we believe that it is a consequence of the modeling since in TRAMOII the layout generation imposes limits on the size of the polysilicon lines (input capacitances) and on the size of the active areas (output capacitances). However, in TROPIC the layout assembly malleability and the compactor processing increase the occurrency of this capacitances.

7 Conclusions and perspectives

The circuits implemented present different performances and sizes, according to the different transistor sizing they have. However, based on the realized experiences, it is possible to see that random logic layout generation using non-conventional methodologies can produce interesting performance/cost ratios when compared with traditional approaches. Cell library limitations, fixed transistor sizing, and other critical points in the Standard Cell methodology can be overcomed with these new methodologies, where each design is carried out according to its specific requirements.

In the environments evaluated there are several research topics for further work. For example, the interaction between TROPIC and TRAMOII modeling avoiding the disadvantages of both and joining its main advantages can contribute to achieve a very efficient layout generator. The research on transparent cell generation and specific technology mapping (exploring the complex gates that can be generated) will also contribute to turn these environments into powerful tools for designing circuits with the desired performance.

We only have considered two metal layer technologies, but when working with the emerging technologies, the presence of more than two metal layers naturally needs the management of the transparency concept. Despite all the existing possibilities, we think that the presented methodologies are also well suited for these technologies.

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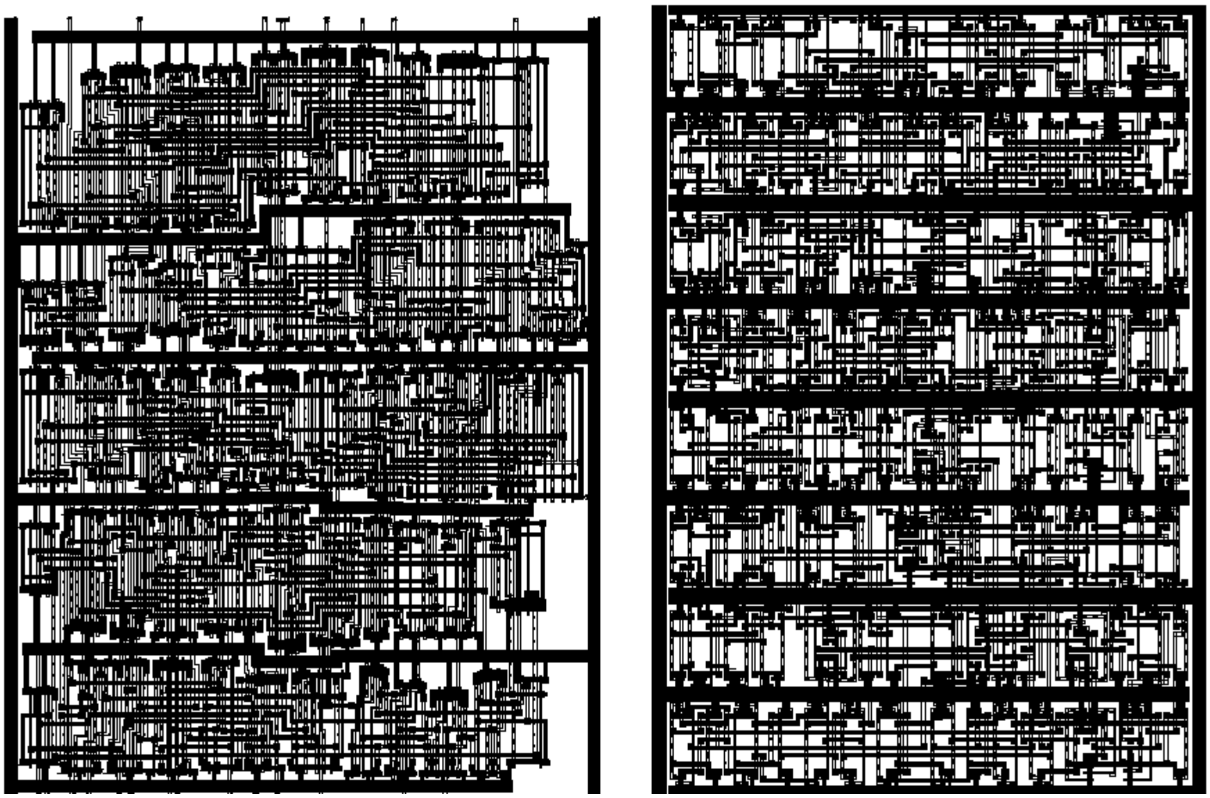

Figure 3: Trpw=T2 and Alu79 circuit layouts

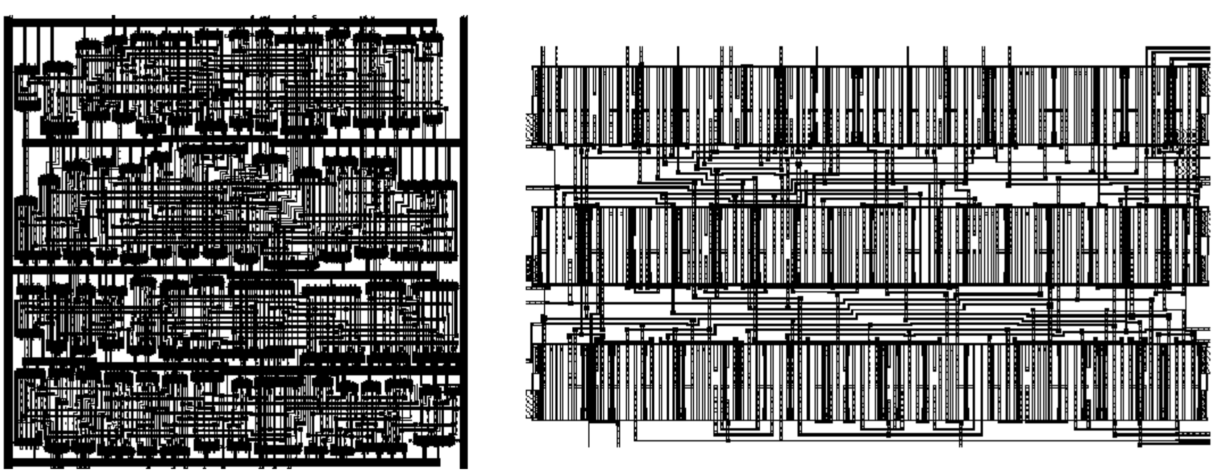

Figure 4: Trpw=T2 and SC1 circuit layouts