A Full Over-the-Cell Routing Model

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Abstract— This paper describes a Full Over-the-Cell routing model to perform circuit connections over the transistors by using "transparent cells". The methodology provides flexibility and the resulting layout style presents interesting performance/cost ratios if compared to those produced by Standard Cell and traditional Over-the-Cell routing models. A Symbolic Environment is shown, where it is possible to make the routing over real cell layouts, based on a restriction matrix. Some special routing techniques are mentioned and practical results are shown.

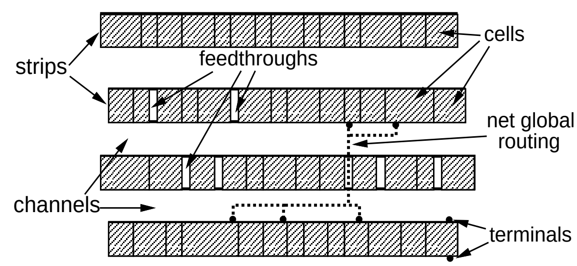

Fig. 1. Standard Cells circuit structure.

I. Introduction

With the increase in VLSI circuits complexity, it is fundamental the use of improved EDA tools to carry out the design of such circuits. The search for new styles and methodologies for random logic synthesis at the layout level is still an important point, mainly in the presence of new technologies.

The automation cannot penalize the design performance or integration density, but the Standard Cells, the most widely used methodology for random logic generation, leads to a reasonable waste of area, performance, flexibility and power dissipation, due to its fixed topological structure, which is shown in Fig. 1. This structure was introduced because of its simplicity, allowing the automatic generation of several kinds of circuits by using pre-designed cell libraries. However, manually designed circuits usually present a better performance/cost ratio based on different layout structures.

To minimize the waste of area with the Standard Cell routing channels, several techniques were proposed, in which some connections are made over the cells using the layers not yet occupied. This is called Over-the-Cell Routing or OTC [3]. An example of the physical model used for OTC routing is shown in Fig. 2. It is important to note that in Standard Cells with 2 metal layers we do not need feedthroughs because the second metal layer can cross over the cell rows. But if it is used OTC routing, one metal layer must be used for cell design and the second one must be used for the OTC connections. Thus, the feedthroughs are needed, and the reduction on the channel height will not be so good because it will impose the consumption of other resources (horizontal space).

The availability of more than two metal layers has been studied in several ways to improve the OTC routing, and new models for OTC routing and for cell design have been proposed [16] [2] [4], but in all this proposals, the circuit is normally divided into strips and channels, and only part of these channels is minimized by the use of a planar routing (or river routing) over the cells.

In [4] it is mentioned that the authors are currently interested in the possibility of combining the global routing with the OTC routing step since the decision about the position of feedthroughs has significant impact on the routing problem. The authors are also interested in com-

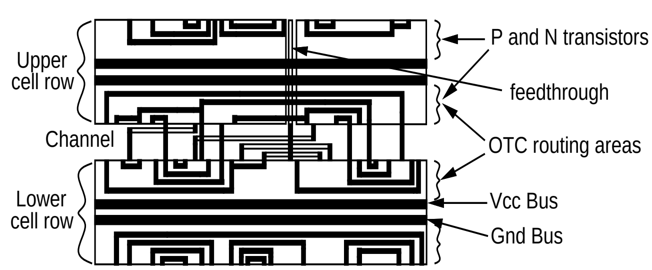

Fig. 2. Physical model for OTC routing.

bining the cell generation with the over-the-cell routing approach together to achieve more efficient utilization of the area over the cells to both intracell and intercell connections. The routing model described in this paper tries to address these two points by exploring a different methodology.

II. The Transparent Cell Approach

The full-custom functional blocks implemented by the microprocessor designers in the 70's were usually made with a different layout structure if compared to Standard Cell circuits. They had a nice density because the routing was normally performed over the transistors' active area, slicing the circuit into strips, limited by the power supply lines, but using no routing channels. This structure also leads to a better global optimization. A similar topology is generally used in the bit-slice datapath generation because the regularity can be exploited with the design of blocks that are replicated and connected by abutment.

The TRANsparent Cell Approach (TRANCA) [11] [12] was proposed based on this observation, and the main goal is to achieve an automatic generation of random logic by using a layout structure with the same characteristics and advantages of the manually designed ones. In this original style, the connections are routed over the cells' active area, as shown in Fig. 3, resulting in an appropriate combination between cell and routing structures.

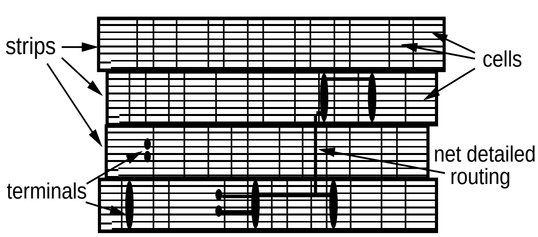

Fig. 3. Transparent Cell circuit structure.

The cells are specially designed to offer transparency for the routing layers. The transparency is the property of a cell or block to be crossed in a specific direction, position, and layer, by an external signal, without any conflict with its internal components. However, instead of considering only the set of possible feedthroughs to cross the cells, the presented methodology extends this simple transparency model to take into account the possibilities of use each routing layer (including contact and vias) in all free positions over the cells.

This can be considered as "detailed transparency", and it can be achieved by designing the cells with all metal elements oriented and aligned according to a virtual grid that represents the positions of horizontal and vertical routing tracks. As it is possible to see in Fig. 4, the cell terminals can be optimally positioned to provide, at the same time, easy external access and good intracell organization.

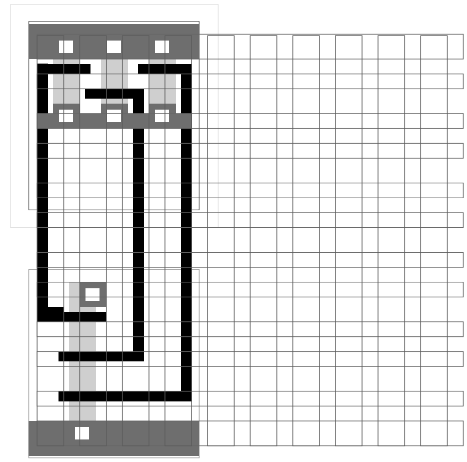

Fig. 4. A nand3 transparent cell

In a two metal technology, the used routing layers are metal 1 running in horizontal direction and metal 2 running in vertical direction. The cell shown in Fig. 4 is transparent for these two metal layers. Fig. 5 shows the steps between adjacent tracks using planar routing (without contacts), using normal grid with contact head spaces, and using alternate contact positions to minimize the waste of area, as it is used in the examples described here.

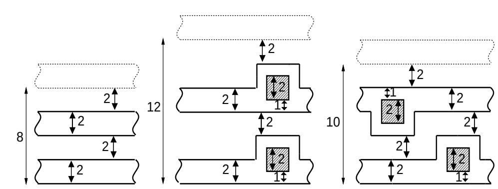

Fig. 5. Tracks spacing according contact positions.

In the proposed methodology it is considered de possibility of transparent cell automatic generation [13], but it is out of the scope of this paper. The TRANCA design methodology is based on the following points:

strip structure - the circuit is composed of cell rows without routing channels among them (Fig. 3);

effective transparency - exploration on the overlapping of routing and cell layouts, minimizing the waste of area with dedicated regions;

malleability - the property of a cell or block to be adapted for different height or width constraints according to the effective transparency;

tracks management - organization in the placement of the segments on the grid to avoid random tracks allocation, providing a good alignment. This must be done to let long free tracks available for long connections.

III. The Full Over-the-Cell Routing Model

The routing problem resulting from the Transparent Cell Approach is defined as "Full Over-the-Cell" Routing model. The word "Full" means that it maximizes the overlapping of the routing over the cell layouts. However, if the routing becomes clearly a limiting factor in large circuits, the insertion of routing dedicated spaces can be used to complete the connections.

The FOTC routing greatly differs from the previous OTC models, where only the remaining layers over the cells are used for routing, not considering transparency in the first metal layer, and using limited access for terminals. Fig. 6 shows the position of a connection between two neighboring cells in a traditional Standard Cell, in a Standard Cell with OTC routing, and in the TRANCA FOTC routing model. Of course, in the last case the cells are not so small, but the position of the connections and the cell elements are optimized together. By using transparency, the interstrip connections are also much less expensive, because they do not need feedthroughs.

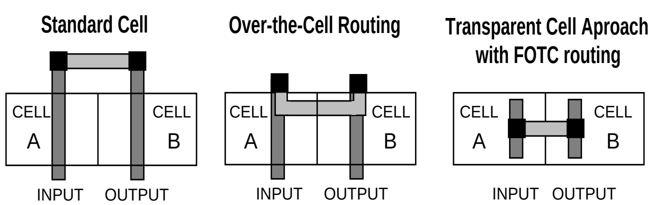

Fig. 6. Connections between neighboring cells.

While in the Standard Cell models the routing problem is naturally divided into well-defined limited sub-problems (channels), the FOTC routing has an uniform distribution over the circuit block, which is composed by the cell layouts without exclusive routing spaces. The connections must be done looking for a detailed routing optimization over the whole over-the-cell circuit area, considering net terminals in the middle of this area and all layout constraints. An important difference from this model is that the routing phase cannot insert spaces in a simple manner, because it is realized over the already placed cell layouts. The advantage is that it will use the maximum overlapping with the cell layouts and directly access cell terminals in its nearest internal points. The main disadvantage of this type of modeling is that it requires a good area estimation with management of some spaces inside the block, when the placement step is done, to guarantee the routing over the defined area. This is like the prediffused approaches, in which the routing has limited area and cannot allocate on-the-fly the needed space.

So, the Transparent Cell Approach can be used to make a Full Over-the-Cell routing that provides layout flexibility and good global/local optimization. To develop module generators with FOTC routing we must consider 3 points: 1 - specific partitioning/placement targets; 2 - integral detailed routing approach; 3 - transparent cell generation.

IV. A Full Over-the-Cell Routing System

Here it is described a system that can handle the FOTC routing as defined above. This system, called MARTE (MAtrix RouTing Environment), was developed for the Marcela [5] and TramoII [8] [10], layout generators, which use a similar 2-layer grid organization. A symbolic FOTC routing can be made using the grid according to restrictions extracted from real cell layouts. The restriction is the information about the constraint or possibility to use each of the routing layers on a specific position over the circuit, and this information is extracted from the layout for each crosspoint between horizontal and vertical grid tracks (symbolic positions).

Fig. 7 shows an example of a transparent inverter cell, with its extracted restriction matrix, and a simple routing between two inverters, where we can see the symbolic abstraction used for the routing. The output of the first inverter connects to the input of the second one. The output of the last one is only routed to connect its P and N parts, which are separated in the cell layout to simplify the connection with neighboring cells.

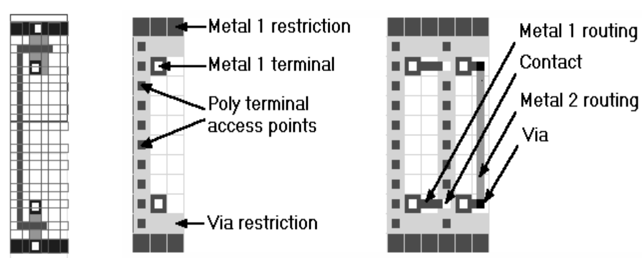

Fig. 7. Symbolic abstraction used for routing.

At this time we are using a set of variations of the Lee's maze router as the first implemented algorithm in the system. This choice was made in function of the great amount of information to be managed due to the TRANCA restrictions and the generality of this technique. To minimize the constraints concerning to the performance of Lee's algorithm in large problems, a set of improvements were applied [7]. The main improvements used are: net ordering; research space restriction [15]; and free orientation, not obeying the layers restricted directions in the last routing trials.

Some particular adaptations and techniques were also developed to provide an adequate FOTC routing, what provides an improvement on the maze router quality too. The techniques that are relevant to the FOTC routing are mentioned in the following subsections, but some of them are specific for the maze router algorithm when used in this model.

A. Multipoint terminals

Multipoint origin and multipoint targets are used for maze router expansion step to do a detailed modeling of the terminals access, because in the TRANCA model the terminals are not restricted to only one grid point or to a regular position (Fig. 7). The routing input and output files use the same syntax and semantics. So, after a partial routing, all the connection path points can be used as origin or target points.

B. New path coding

A new path coding scheme must be used to provide correct expansion and retrace for multipoint terminals with a minimum memory requirement. The sequence proposed in [1] cannot be directly used for multipoint origin (Fig. 8a), because in the Akers' code we cannot distinguish if we are searching toward the origin or toward the target. To solve this problem we use a modified sequence based on the same idea. We use code repetition but with two bits per code instead of only one. The sequence 001122330011... provides the expected solution with the use of one backtracking level (Fig. 8b).

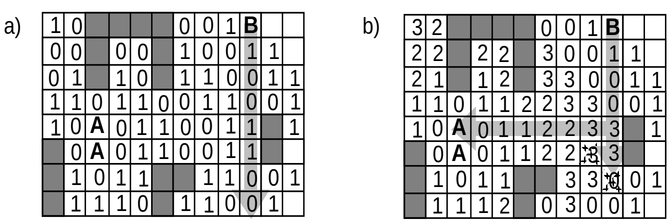

Fig. 8. New path coding for multipoint origin.

C. Doglegs Substitution, Shrinking and Dragging

The directions used for the metal lines in the routing are restricted to offer the transparency. Hence, a connection can only change from one track to another track, in the same direction, if it can use the other layer between them and if it is possible to put the necessary vias. Therefore, even when changing between neighboring tracks, it is needed to place two vias and to use the other metal layer. After the normal retrace phase, additional steps are done with the found path, where these subsequent vias are replaced by doglegs using only one metal level, with these new elements being well accommodated in the layout (Fig. 9).

D. Alternative Locks

In our system the cell terminals can be described using the layers unused for routing as we can see in Fig. 7. This is made to let the router to complete all metal and contact access elements in pre-diffused approaches and it is also done to use optional access points. It is a crucial point in the TRANCA style. But to avoid active area and poly terminals from being blocked by other connections over its access points, absolute and alternative locks are placed and they are updated during the maze routing process in such a manner that at last one of the terminal access points is reserved for its connection.

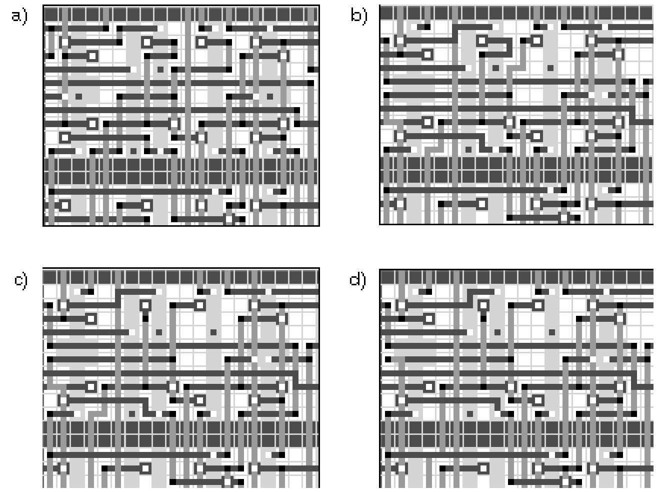

Fig. 9. Doglegs Substitution, Shrinking and Dragging.

V. Practical Results

The MARTE system was used to implement the TRANCA concepts in a well defined symbolic abstraction, in which several system options, characteristics, and algorithms can be experimented. Tables I and II show some data about example circuits generated by using this kind of routing. The circuit "alu80" is composed by library transparent cells according TramoII system, while the other ones have been generated in the sea-of-cells prediffused approach (MARCELA system). Except the circuits alu80 and axis, all the netlists are taken from the ISCAS benchmarks.

The MARCELA circuits have been placed on the minimum matrix portion in which its cells can be assigned to test the routing capacity of the prediffused transistor matrix under consideration (MAR1000). It is possible to see that the routing percentage is about the same for the combinatorial circuits (c beginning names) in despite of the circuit size. This is not true for the sequential ones.

Table II shows the sum of all horizontal and vertical connections made or remaining after the routing of some circuits. It is also shown the restriction matrix filling obtained and needed to complete the routing in both metal layers.

When the routing becomes a limiting factor a large circuit area must be used to make the routing over. In the prediffused approaches, it means that we need to use a large matrix portion, while in the cell based generators

TABLE I
ROUTING INFORMATION ABOUT SOME CIRCUIT EXAMPLES.

Cir-cuit	matrix size	matrix trans.	used %	connec-tions	routing %
alu80	62x96	422	100.0	302	100.0
s386	168x216	1728	67.25	1050	99.52
axis	182x312	2704	59.10	2054	97.42
s1494	350x408	6800	63.65	3657	94.75
c432	224x216	2304	52.69	966	99.59
c1908	406x456	8816	39.47	2829	99.93

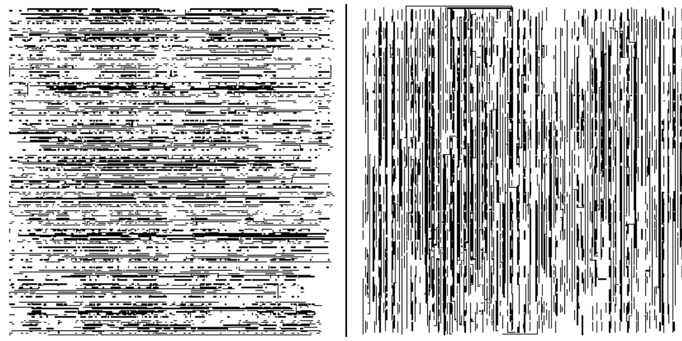

Fig. 10. Metal layers density of a sea-of-cells circuit.

we need to insert appropriate spaces and/or small channels. This indicates the need of further analysis on how to estimate and how to manage the circuit area to solve the problem on the FOTC model.

TABLE II
ROUTING LENGTH AND MATRIX OCCUPATIONS

Cir-cuit	level orient	routing made	filling obtained	routing needed	total filling
alu80	M1 H	2616	68.88%	0	68.88%
	M2 V	2362	37.28%	0	37.28%
axis	M1 H	25500	59.73%	3506	65.91%
	M2 V	33797	58.26%	7535	71.53%
s1494	M1 H	73183	66.65%	26043	84.89%
	M2 V	86403	59.49%	31085	81.26%
c1908	M1 H	68799	53.53%	113	53.60%
	M2 V	90849	48.35%	158	48.44%

Fig. 10 shows the 2 metal layers of the **axis** circuit routing. It was generated according to the sea-of-cells approach, and it is possible to see the routing complexity and its distribution over the prediffused matrix portion. Fig. 11 shows the initial restriction matrix and the complete FOTC routing of the **alu80** circuit. The final layout of this circuit presents an integration density of about 3440 transistors/mm2 in the ES2 1.2 micra technology. The same circuit implemented according to a Standard Cell methodology (with Cadence Edge 2.1) presents an integration density of about 3028 transistors/mm2 using the same technology [9].

VI. CONCLUSIONS AND CURRENT RESEARCH

We have defined the FOTC model to perform the routing over the transistors by using dedicated transparent cells. Since the cells considered in the examples were designed according to automatic generation guidelines, it is possible to develop module generators that produce very interesting results such as a good integration density and an adequate transistor sizing to match design constraints and performance specifications. The possibility of generating complex gates can also reduce the number of transistors in about 30% to 40%. It cannot be done in the Standard Cell approach with the limitation of cell libraries.

The routing model is adequate to optimize at the same time local and global aspects of cell and routing structures. We are currently researching how to improve the routing performance and how to generate large circuit blocks with more efficiency. The net ordering and CPU time problems with maze routers must be overcommed, and a key idea is the use of a global approach to the problem. But the use of a normal global routing step with the same detailed algorithm will not be able to solve the CPU time, memory consumption and ordering problems of the maze routers, for example.

So, it is under development a new algorithm for FOTC to optimize the entire circuit routing problem instead of considering the routing of a connection at a time. It is based on some ideas taken from the channel routing algorithms, which presents good resource utilization, but considering the generality and the constraints of the FOTC model. The routing completeness is clearly the main goal, but we are looking for the tracks occupation using a parallel approach as a way for improving the results.

For new technologies with more than 2 or 3 metal layers the search for new routing structures for module generation becomes an important point. The research on transparency will be useful mainly because there is no more necessity to continue separating the cell rows with dedicated routing channels.

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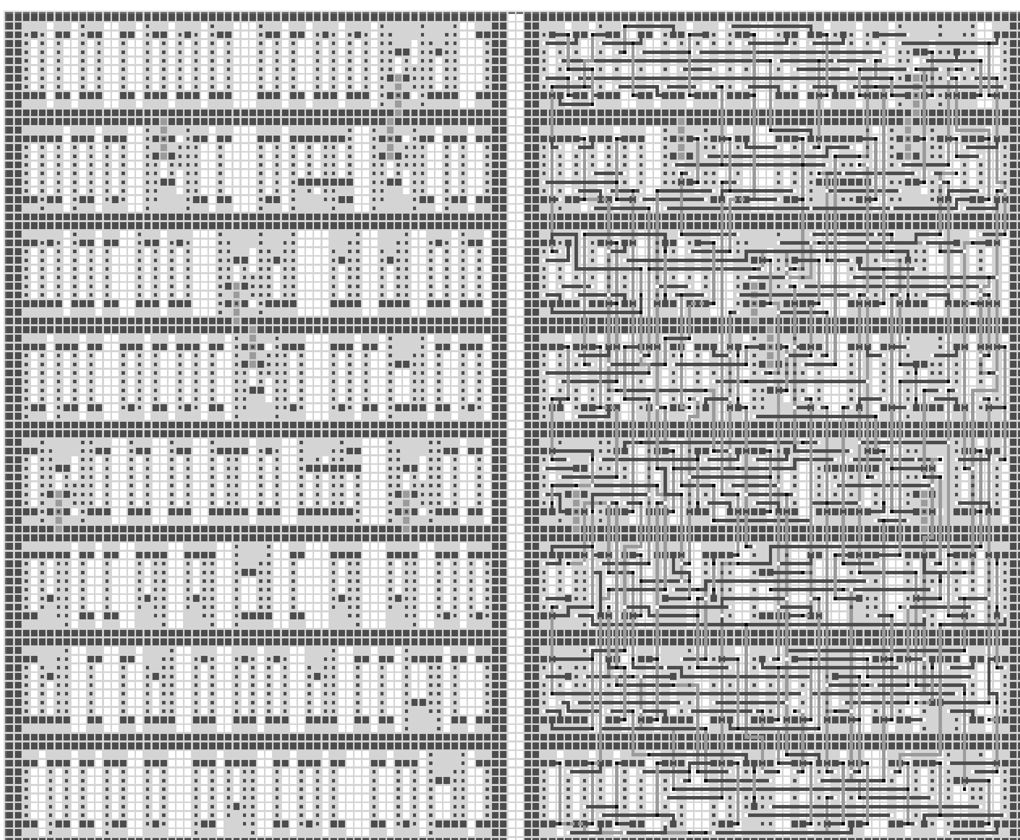

Fig. 11. TRAMOII symbolic routing example.

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